Proceedings of the 35th Workshop on Compound Semiconductor Devices and Integrated Circuits

Catania (Italy), May 29th - June 1st , 2011

WOCSDICE 2011

Edited by: Vito Raineri and Fabrizio Roccaforte

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Welcome to WOCSDICE 2011

You are warmly welcome to the 35th Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE 2011, in Catania, Italy. The conference is organized by the Institute for Microelectronics and Microsystems of the National Research Council (IMM-CNR).

WOCSDICE 2011 is held in the picture gallery ("Pinacoteca") of the Diocesan Museum of Catania, situated in the ancient seminar ("Seminario dei Chierici") of the Cathedral, in the heart of the old town.

The aim of the 35th Workshop on Compound Semiconductor Devices and Integrated Circuits is to bring together internationally recognised researchers, young scientists and engineers to present state-of-the-art research findings in the areas of compound semiconductors, devices and integrated circuits. In these fields, an intense activity is currently carried out in Catania, thanks to the cooperation between IMM-CNR, University, industries and private research centres.
The workshop welcomes researchers from universities and research institutions, and scientists and engineers working in industry, from more than 20 countries.

The organizers maintained the tradition of an intensive and informal scientific discussions and interactions between young researchers and experts in the field.
In the scientific program, a special emphasis was given to III-V compounds and large-area scaling; III-nitride materials, devices, for both optoelectronics and power electronics, and related reliability aspects; high-frequency circuits and optical interconnects. The focus was extended also towards advanced devices on organic semiconductors and novel materials like graphene.

A special thank must be given to all the invited speakers and to the regular participants, that through their precious contributions guaranteed the high scientific level of the conference. The conference sponsors are greatly acknowledged for their important support.
Finally, we thank everyone who helped to arrange WOCSDICE 2011.

On behalf of the local organizing committee, we would like to welcome all of you and wish you a pleasant and fruitful stay in Catania.

Vito Raineri
Fabrizio Roccaforte

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Scientific Program WOCSDICE 2011

Sunday May 29th 2011

17:00-19:00 **Registration**
19:00-20:30 **Welcome Reception**

Monday May 30th 2011

8:00 **Registration**
8:20-8:40 **Welcome and Conference Opening**

Session 1 **(In,Ga)As devices and In(P,Sb) devices**
(Chair Prof. Hans Hartnagel - TU Darmstadt, Germany)

8:40-9:00 **Franco Giannini** (University of Tor Vergata, Roma, Italy)
Invited *Being Seventy-five still Young: The Doherty Power Amplifier*
9:00-9:10 **Ion Oprea** (Technische Universität Darmstadt, Germany)
Analysis of thermal dissipation for mm-wave frequency multipliers using GaAs Schottky Diodes
9:10-9:20 **Benedetto Pasciuto** (University of Tor Vergata, Roma, Italy)
Advanced PHEMT GaAs E/D technology, modeling and characterisation
9:20-9:30 **Andrea Bentini** (University of Tor Vergata, Roma, Italy)
C-Band MMIC Chipset and Digital Control Circuits for T/R Modules based on GaAs Enhancement/Depletion Technology
9:30-9:40 **Paolo Romanini** (Selex Sistemi Integrati SpA, Roma, Italy)
High level of automated process for Broadband and X-band MMIC's production
9:40-9:50 **Giuseppe Moschetti** (Chalmers University of Technology, , Goteborg, Sweden)
Anisotropic transport of InAs/AlSb heterostructures grown on InP substrates
9:50-10:00 **Werner Prost** (University Duisburg-Essen, Germany)
Sample-and-hold circuits using InAs nanowire FETs
10:00-10:10 **Andreas Westlund** (Chalmers University of Technology, Göteborg, Sweden)
Fabrication and characterization of InGaAs slot diodes
10:10-10:20 **Koichi Maezawa** (University of Toyama, Japan)
Characterization of InSb MOS diodes on Si substrates prepared by surface reconstruction controlled epitaxy
10:20-10:30 **Mirja Richter** (IBM Research – Zurich, Switzerland)
Development of (In,Ga)As-MOSFETs: High-k gate stacks and options for integration on silicon

10:30-11:00 ***COFFEE BREAK***

Session 2 **Microwaves and terahertz devices and technology**
(Chair Prof. Dimitris Pavlidis - TU Darmstadt, Germany)

11:00-11:20 **Roger A. Lewis** (University of Wollongong, Australia)
Invited *Terahertz generation in compound semiconductors*
11:20-11:30 **Daniel Schönherr** (Technical University Darmstadt Germany)
Electro-optic detection of continuous wave THz radiation
11:30-11:40 **Hans Hartnagel** (Technical University Darmstadt Germany)
Microwave Circuits affected by Passive Inter-Modulation in Communication Satellites
11:40-11:50 **Farid Medjdoub** (IEMN, Villeneuve d'ascq, France)
SiN/AlN/GaN: A promising heterostructure for millimeter wave applications
11:50-12:00 **Jonathan Felbinger** (Chalmers University of Technology, Göteborg, Sweden)
$Al_{0.5}Ga_{0.5}N$/AlN/GaN HEMTs for Microwave Applications
12:00-12:10 **Judith Spiegel** (Chalmers University of Technology, Göteborg, Sweden)
Design and characterization of GaN HEMT varactors for reconfigurable MMICs

12:10-12:20 **Grigory Simin** (University of South Carolina, Columbia, USA)
Power III-Nitride devices with frequency-configurable elements

12:20-12:30 **Cezary Sydlo** (Technische Universität Darmstadt, Germany)
Demonstration of RTD oscillations beyond tunnel-lifetime limit

12:30-12:40 **Moumita Mukherjee** (University of Calcutta, India)
Full-Scale Non-Linear Analysis of III-V Nitride Based Transit Time Diode for High-Power Generation in the Terahertz Regime

12:40-13:00 **Mircea Dragoman** (IMT, Bucharest, Romania)
Invited *Graphene devices for microwaves and terahertz applications*

13:00-14:30 ***LUNCH***

Session 3 **Graphene and carbon nanostructures**
(Chair Prof. Luigi Colombo - Texas Instruments Incorporated, Dallas Tx, USA)

14:30-14:50 **Phaedon Avouris** (IBM T.J.Watson Research Center, Yorktown Heights, USA)
Invited *Fast graphene electronics and photonics*

14:50-15:00 **Filippo Giannazzo** (CNR-IMM, Catania, Italy)
Epitaxial graphene on off-axis 4H-SiC (0001): study of the growth mechanisms and nano/micro-scale electrical characterization

15:00-15:10 **Antonino La Magna** (CNR-IMM, Catania, Italy)
Coherent Electron Transport in quasi one-dimensional carbon-based systems

15:10-15:20 **Giuseppe Angilella** (Dipartimento di Fisica e Astronomia, Università di Catania, Italy)
Strain effects on the electronic properties of graphene

15:20-15:30 **Ioannis Deretzis** (CNR-IMM, Catania, Italy)
Theoretical investigation of the structural, electronic and transport properties of pure and intercalated graphene on SiC substrates

15:30-15:40 **Kostantinos Zekentes** (IESL- FORTH, Heraklion, Crete, Greece)
SiC nanowire FET operation improvement by using Schottky contacts at source and drain regions

15:40-15:50 **Kazuhiko Matsumoto (**Osaka University, Japan)
1/10 low bias operation and individual charge detection of carbon nanotube quantum nano memory

15:50-16:00 **Oktay Yilmazoglu** (Department of High Frequency Electronics, TU Darmstadt, Germany)
Flexible carbon nanotube arrays for pressure sensing with high spatial resolution

16:00-16:30 ***COFFEE BREAK***

Session 4 **Graphene devices**
(Chair Prof. Phaedon Avouris - IBM T.J.Watson Research Center, USA)

16:30-16:50 **Luigi Colombo** (Texas Instruments Incorporated, Dallas Tx, USA)
Invited *Graphene for Beyond Scaled CMOS*

16:50-17:00 **Shabnam Shambayati** (ECE Dept., University of British Columbia Vancouver, Canada)
Performance predictions for Graphene-Window Schottky-barrier solar cells

17:00-17:10 **Dong Hao** (Cornell University, Ithaca, NY, USA)
Covalent Functionalization of Graphene Towards a Biological Transducer

17:10-17:20 **Tetsuya Suemitsu** (RIEC, Tohoku University, Japan)
Graphene FETs with SiCN gate stack deposited by PECVD using HMDS vapor

Session 5 **Thermal effects, reliability and packaging issues**
(Chair Prof. Gaudenzio Meneghesso – University of Padova, Italy)

17:20-17:30 **Yvon Cordier** (CRHEA-CNRS, Valbonne, France)
Effects of substrate and buffer layer quality on the behavior of AlGaN/GaN HEMTs : thermal effects versus electron trapping

17:30-17:40 **Milan Ťapajna** (CDTR, University of Bristol, UK)
The Impact of Barrier Surface Treatment on AlGaN/GaN HEMT Reliability

17:40-17:50 **Nicole Killat** (CDTR, University of Bristol, UK)
Thermal Challenges of Wafer Bonding of AlGaN/GaN HEMTs

17:50-18:00 **Cristina Miccoli** (ST Microelectronics, Catania, Italy)
Two-Dimensional Transient Simulations Including Trapping and Thermal Effects in GaN HEMTs

18:00-18:10 **Abel Fontserè** (IMB-CNM-CSIC, Barcelona, Spain)
Reverse Current Thermal Activation of AlGaN/GaN HEMTs

18:10-18:20 **Enrique Miranda** (Universitat Autònoma de Barcelona, Spain)
Extraction of the degradation parameters of constant voltage- stressed Al/HfYO$_x$/GaAs structures with important series resistance effects

18:20-18:30 **Harald Etschmaier** (Infineon Technologies Austria AG, Villach, Austria)
Characterization of the phase composition and Microstructure in diffusion soldered Au/Sn joints for die attach

18:30-18:40 **Alessio Pantellini** (SELEX Sistemi Integrati, Roma, Italy)
Thermal Assessment of AlGaN/GaN on 50µm Silicon Microstrip Technology

18:40-18:50 **David Maier** (Institute of Electron Devices and Circuits, University of Ulm, Germany)
Large Signal Operation of InAlN/GaN HEMTs at Very High Temperature

18:50-19:00 **Arvydas Matulionis** (Semiconductor Physics Institute of CPST, Vilnius, Lithuania)
Mitigation of hot-phonon effects in a twin channel for a GaN heterostructure field effect transistor

Tuesday May 31^{tst} 2011

Session 6 **Challenges and perspectives**
(Chair Prof. Petra Specht - University of California at Berkeley, USA)

9:00-9:20 **Gaudenzio Meneghesso** (Department of Information Engineering, University of Padova, Italy)
Invited *Report on 47th Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD 2011): challenges for compound semiconductors*

9:20-9:40 **Antonino Scuderi** (ST Microelectronics, Catania, Italy)
Invited *GaN and SiC from industrial perspectives*

Session 7 **Nitrides: materials and processing**
(Chair Prof. Takashi Mizutani - Nagoya University, Japan)

9:40-10:00 **Michał Leszczynski** (Unipress and TopGaN Ltd, Warsaw, Poland)
Invited *Influence of substrate miscut on properties of GaN-based devices*

10:00-10:10 **Mariusz Martyniuk** (The University of Western Australia, Australia)
Mechanical properties of lateral epitaxial overgrown gallium nitride

10:10-10:20 **Hideo Kawanishi** (Dept. Electronics Engineering, Kogakuin University, Japan)
Carbon-doped p-type (0001) plane AlGaN (Al= 0.06 to 0.50) with high hole density

10:20-10:30 **Giuseppe Greco** (CNR-IMM, Catania, Italy)
Carrier transport in inhomogeneous annealed Au/Ni/p-GaN interfaces

10:30-10:40 **Ales Chvála** (Department of Microelectronics, University of Technology, Bratislava, Slovakia)
Analysis of the leakage current of AlGaN/GaN Schottky diode dependent on ohmic contact pad electrode position

10:40-10:50 **Berndt Schineller** (AIXTRON SE, Herzogenrath, Germany)
Process Stability Study of Mass Production of LED Structures by MOCVD

10:50-11:00 **Yury Buzynin** (Institute for Physics of Microstructures -RAS, Nizhny Novgorod, Russia)
InN, AlN, GaN films on fianite substrate and buffer layer

11:00-11:30 ***COFFEE BREAK***

Session 8 **GaN HEMT devices**
(Chair Prof. Elias Muñoz - Universidad Politécnica de Madrid, Spain)

11:30-11:50 **Peter Kordoš** (Department of Microelectronics, University of Technology, Bratislava, Slovakia)
Invited *Preparation and properties of GaN-based MOSHFETs*

11:50-12:00 **Philipp Leber** (Institute of Electron Devices and Circuits, Ulm University, Germany)

Influence of Passivation on the Gate Leakage Current Behavior of AlGaN/GaN High Electron Mobility Transistors

12:00-12:10 **Herwig Hahn** (GaN Device Technology, RWTH Aachen University, Germany)
Influence of oxygen addition in SiN dry etch process on device characteristics of passivated AlGaN/GaN HFETs

12:10-12:20 **Alessandro Chini** (University of Modena and Reggio Emilia, Italy)
Dependence of static and dynamic GaN HEMT characteristics from Fe-doped GaN buffer parameters

12:20-12:30 **Donatella Dominijanni** (CNR-IFN, Rome, Italy)
Scalable Gate two EBL steps fabrication process for optimal high frequency GaN HEMT performances

12:30-12:40 **Dominik Schrade-Köhn** (Institute of Electron Devices and Circuits, Ulm University, Germany)
Impact of Ar-milling on the GaN surface and correlation with electrical results on AlGaN/GaN HEMTs

12:40-12:50 **Nico Ketteniss** (GaN Device Technology, RWTH Aachen University, Germany)
Impact of gate length on the device performance of passivated InAlN/GaN HFETs

12:50-13:00 **Alexander Alexewicz** (TU Wien, Austria)
Threshold voltage scaling in E-mode InAlN/AlN GaN-HEMTs on Si substrate

13:00-13:10 **Antonio Stocco** (Department of Information Engineering, University of Padova, Italy)
Electrical and reliability investigation of AlGaN/GaN HEMTs grown on 8° off-axis 4H-SiC

13:10-14:40 ***LUNCH***

14:40-24:00 ***TRIP TO TAORMINA AND SOCIAL DINNER* (suggested dresses: casual)**

Wednesday June1tst 2011

Session 9 **WBG compound semiconductors for power electronics**
(Chair Prof. Kostantinos Zekentes - IESL-FORTH, Greece)

9:00-9:20 **T. Paul Chow** (Rensselaer Polytechnic Institute, Troy, NY, USA)
Invited *Recent Advances in High-Voltage GaN MOS-gated Transistors for Power Electronics Applications*

9:20-9:30 **Takashi Mizutani** (Nagoya University, Japan)
Normally-off mode AlGaN/GaN HEMTs with p-InGaN cap layer

9:30-9:40 **Rimma Zhytnytska** (FBI, Leibniz Institut für Höchstfrequenztechnik, Berlin, Germany)
High voltage power transistor design– influence of metallic contact area on device breakdown

9:40-9:50 **Eldad Bahat-Treidel** (FBI, Leibniz Institut für Höchstfrequenztechnik, Berlin, Germany)
AlGaN/GaN/GaN:C back barrier Schottky diodes for power switching

9:50-10:00 **Olivier Menard** (ST Microelectronics, Tours, France)
Progresses in GaN Power Rectifier

10:00-10:10 **Alessia Frazzetto** (CNR-IMM, Catania, Italy)
Impact of surface processing on the electrical properties of p-type implanted 4H-SiC for power devices

10:10-10:20 **Aurore Constant** (IMB-CNM-CSIC, Barcelona, Spain)
Performance and bias temperature instability characteristics of 4H-SiC MOSFETs with nitrided gate oxide grown by RTP

10:20-10:50 ***COFFEE BREAK***

Session 10 **Optoelectronics, detectors and sensors**
(Chair Prof. Joachim Würfl - FBI für Höchstfrequenztechnik, Germany)

10:50-11:10 **Jean-Yves Duboz** (CRHEA, CNRS, Valbonne, France)
Invited *AlGaN based arrays for Extreme UV detection*

11:10-11:20 **Elias Muñoz** (Univ. Politécnica de Madrid, Madrid, Spain)
(In,Ga)N Photodetectors and Applications in Biophotonics

11:20-11:30 **Laurent Ottaviani** (University Paul Cézanne, Marseille, France)

Influence of p+ layer parameters on 4H-SiC UV PiN Photodetector characteristics

11:30-11:40 **Stefan Herbert** (RWTH, Aachen University, Germany)
Challenges of high-speed EUV mask blank inspection

11:40-11:50 **Matteo Dal Lago** (Department of Information Engineering, University of Padova, Italy)
The role of operating conditions in the chip-level degradation of white LEDs

11:50-12:00 **Jens-Peter Biethan** (Department of High Frequency Electronics, TU Darmstadt, Germany)
MOCVD grown ZnO on c-plane sapphire substrates for light and gas sensing applications

12:00-12:10 **Clifton J. Fonstad** (MIT, Cambridge, MA, USA)
Multi-waveguide Needle Probes and Integrated Laser Diodes for Opto-genetic Neural Applications

12:10-12:20 **David J.Y. Feng (**National University of Kaohsiung, Taiwan)
All-in-one design of integrated 1x2 TE/TM polarization splitter/combiner/converter on InGaAlAs-InP

12:20-12:30 **Aris Christou** (University of Maryland College Park, Maryland USA)
Dielectric Constants With Extended Model of Interband Transition Contributions for AlGaInAs Quaternary Semiconductor Alloys

12:30-12:40 **Carlo De Santi** (Department of Information Engineering, University of Padova, Italy)
Electro-Optical analysis of the degradation of advanced InGaN-laser structures

12:40-12:50 **Alexander Buzynin (**A.M. Prokhorov General Physics Institute, RAS, Moscow, Russia)
Functional fianite films in photonics

12:50-14:30 ***LUNCH***

Session 11 **Miscellaneous: novel materials, devices, and applications**
(Chair Prof. David Pulfrey - University British Columbia, Canada)

14:30-14:40 **Irina Khmyrova** (University of Aizu, Japan)
Resonant MEMS with two-dimensional electron gas system

14:40-14:50 **Alexander V. Luce** (University of California at Berkeley, USA)
MBE Grown Self-Catalyzed III-V Nanowires on Silicon

14:50-15:00 **Carlos García Núñez** (Universidad Autónoma de Madrid (UAM), Spain)
High mobility n-type Zn3N2 thin films as channel for thin film transistors

15:00-15:10 **Petra Specht** (University of California at Berkeley, USA)
Low Dose Microscopy of Semiconducting and Metallic Nanostructures: Towards Recovering Original Material Structures

15:10-15:20 **Antonella Sciuto** (CNR-IMM, Catania, Italy)
Interdigit 4H-SiC Vertical Schottky Diode for Beta-Voltaic Applications

15:20-15:30 **Davide Spirito** (Dipartimento di Fisica, Università degli Studi Roma Tre, Roma, Italy)
Spin properties and ballistic transport in low-dimensional AlGaN/AlN/GaN systems

15:30-15:40 **Daniel Slocombe** (Cardiff University, School of Engineering, UK)
Dielectric relaxation of transparent conducting oxides at microwave frequencies

15:40-15:50 **Patrick Fiorenza** (CNR-IMM, Catania, Italy)
High capacitance density capacitors by calcium copper titanate thin films

15:50-16:00 **Ibrahim Abdel-Motaleb** (Northern Illinois University, DeKalb, IL USA)
Investigation of the behavior of barium strontium titanate MOS capacitors

16:00-16:10 **Roman Vitushinsky** (Holst Centre, Eindhoven, The Netherlands)
AlGaN ultrathined 2DEG structures for NOx sensing

16:10 **Closing Remarks**

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Session 1 :

(In,Ga)As devices and In(P, Sb) devices

Chair : Prof. Hans Hartnagel

Monday May 30, 08:40 - 10:30

BEING SEVENTY-FIVE STILL YOUNG: THE DOHERTY POWER AMPLIFIER

P. Colantonio, F. Giannini, R. Giofrè*, L. Piazzon

Electronic Engineering Department, University of Tor Vergata, via del Politecnico 1, Roma, Italy
* E-mail: giofr@ing.uniroma2.it

ABSTRACT

In this contribution, the evolution of the Doherty Power Amplifier (DPA) through its first seventy-four years is presented. The aim is to explain why this architecture is still on the wave to realize very advanced power amplifier stages for wireless systems. To this purpose, a reviewing of the DPA principle of operation together with a benchmark of the *state of the art* results, realization methods and fields of application is reported.

1. INTRODUCTION

The idea behind the power amplifier architecture that nowadays is identified as Doherty Power Amplifier has been proposed to the world by W. H. Doherty, many decades ago. The original paper, entitled "*A new high efficiency power amplifier for modulated waves*" was published in the far September, 1936 [1]. Thus, the DPA has just celebrated its first seventy-five years of age.

The last sentence of that old paper was: "*The new amplifier is believed to offer a most logical and practical solution to the problem of efficient operation of high power transmitters"*[1]. The presage done by W. H. Doherty with these few words came true. In fact, even though actual systems are extremely different with respect to the first broadcasting transmitters, in terms of active device technologies, required power levels and adopted modulation schemes, the DPA seems to remain the best candidate to realize power amplifier (PA) stage for modern and future generations of wireless systems.

In fact, the increasing complexity of modulation schemes, used to achieve higher and higher data rate transfer, is asking for PAs able to manage signals with a large time-varying envelope. The resulting peak-to-average power ratio (PAPR) of the involved signals critically affects the average efficiency achievable with traditional PAs. As schematically reported in Fig. 1, such high values of PAPR imply a large back-off operating condition, dramatically reducing the average efficiency levels attained by using traditional PA solutions. In order to stress this effect, it is useful to refer to an ideal Class B PA, delivering an efficiency of 78.6% at its maximum output power, while only 25% at 10dB of back-off. Therefore, when dealing with an amplitude modulated signal, it is more practical to refer to the average efficiency, which is defined as the ratio of the average output power to the average supply DC power. Clearly the average efficiency depends on both the PA instantaneous efficiency and the probability density function (PDF)of the signal. Therefore, to obtain high average efficiency when time-varying envelope signals are used, the PA should work at the highest efficiency level in a wide range of its output (i.e. input) power.

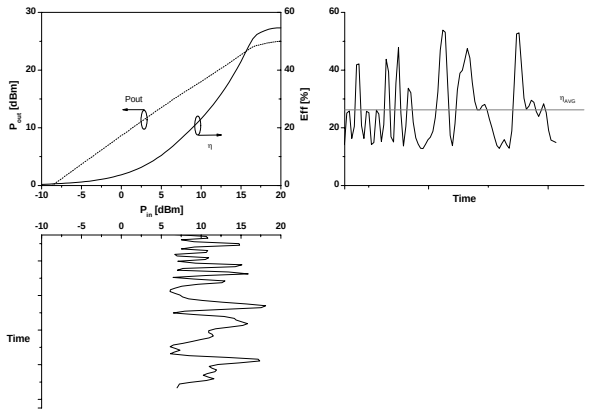

Fig. 1: Average efficiency using traditional PA.

This kind of requirement represents the main feature of the DPA architecture, whose theoretical efficiency behavior is reported in Fig. 2. The region with almost constant efficiency identifies the DPA Output Back-Off (OBO) range, and it is usually fixed according to the PAPR of the signal to be amplified.

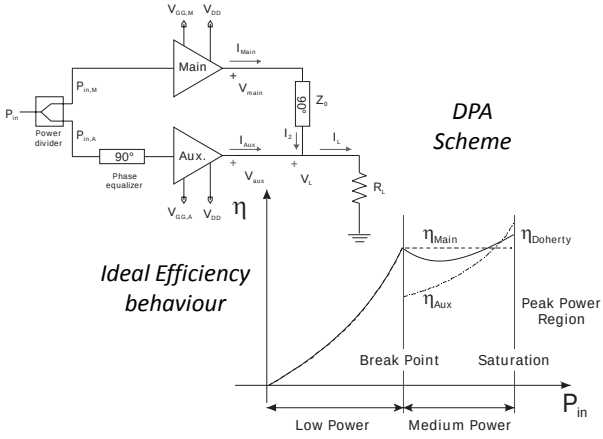

Fig. 2: Typical DPA efficiency behavior *vs.* output power.

2. DPA APPROACHES

As shown in Fig. 2, the typical DPA is composed by two active devices, namely Main and Auxiliary, an impedance inverter network (IIN), a phase compensation network (PCN) and an uneven input power splitter (IPS).

The DPA is based on the idea to modulate the load of the Main device, in order to force it to operate at its maximum efficiency condition for a pre-determined

range of input power levels. Such an action is performed by exploiting the active load concept, by using the Auxiliary device and exploiting the IIN properties. According to this solution, a suitable current supplied by the Auxiliary amplifier in the output load dynamically modulates the load seen by the Main device, coherently with the input power levels.

In the first DPA implementation [1], both devices were biased in Class B condition (hereafter referred as B-B DPA). However, the B–B configuration implies the critical issue to maintain the Auxiliary off along the entire low-power region, which solution was left to "one of the many practical solutions", as indicated in the original Doherty paper [1]. Consequently, it becomes mandatory to complicate the hardware implementation using a switching circuitry to control the on-off Auxiliary condition. In order to avoid such criticisms, a proper Class C bias condition for the Auxiliary device has been adopted. However, in this case, the input power splitter dimensioning becomes a further critical design key aspect [21].

Finally, a pure Class B bias condition for the Main device does not seem to be advisable due to the large cross-over distortion. To avoid this further drawback, a Class AB bias condition for the Main is preferred, resulting in a small reduction of the efficiency as compared as to a pure Class B, but with a significant improvement in the overall linearity.

Nowadays, the actual DPAs employ Class AB (Main) and Class C (Auxiliary) bias conditions (hereafter referred as AB-C DPA). Consequently, the characteristics and values of each DPA elements have to be carefully dimensioned and designed since they are strictly related each other.

Thanks to the huge work done by scientific community, several innovations regarding the DPA have been introduced and validated, mostly devoted to find advanced design methodologies to increase the achievable DPA performances. As example, the existing theoretical gap between the B-B DPA and the AB-C DPA has been filled in [16]. In particular, in this paper it has been highlighted and clarified the role of each elements used in a typical DPA architecture and how they have to be dimensioned considering their mutual dependence..

3. BENCHMARK OF THE STATE OF THE ART

Fig. 3 reports the number of scientific papers focused on DPA architecture over the years, from 2000 to 2010. From it, it is possible to have an idea on the increasing attention to the DPA architecture in the last few years. In fact, in the 2000 only few papers have been published on DPA while in the 2010 at list 65 scientific papers have been published by journal edited by IEEE and Wiley.

In order to benchmark the DPA architecture, an extensive data base with more than 50 scientific papers has been created. However, to avoid exceeding the article maximum length, it was possible to report only a selection of it [2-20] (see Table 1). From the collected data, it is evident that the DPA architecture is usually adopted in telecommunication systems for both handsets and base station terminals. In particular, it is frequently employed in UMTS and WiMax systems and, with minor rate, in WiFi, WLAN, WiBro, and LTE applications. Such observation is also confirmed by Fig. 4 where the number of realizations found in literature are classified as a function of their frequency band.

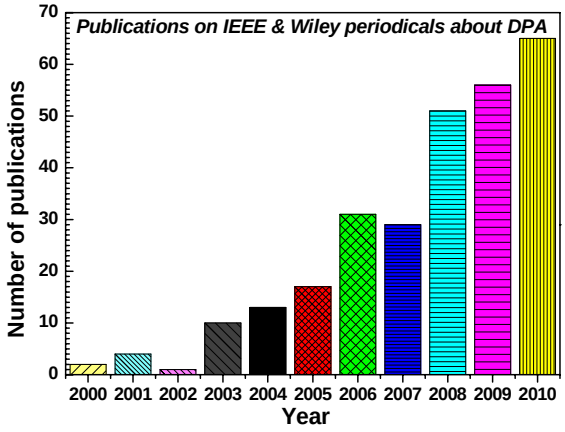

Fig. 3: DPA publications vs. years.

ID	Freq. [GHz]	Pout@ sat [dBm]	η@sat [%]	Gain [dB]	Tecnology.	MMIC Hybrid
[2]	7	38	46	7	GaN	M
[3]	10	30	47	6,5	GaAs	M
[4]	20	23	32	8	GaAs	M
[5]	2,1	38	76	10	GaN	H
[6]	2,5	54	63	11	GaN	H
[7]	2,14	43	47	11	GaN	H
[8]	2,14	39	51	6	GaN	H
[9]	2,5	47	54	10	GaN	H
[10]	1,9	27	65	12	GaAs	H
[11]	2,14	34,7	54	3,5	GaN	H
[12]	2,14	35	54,7	4	GaN	H
[13]	9,6	31	48	6	GaAs	M
[14]	2,14	37	58	9	GaN	H
[15]	3,5	51	37	7,5	GaN	H
[16]	2,14	36	70	7,5	GaN	H
[17]	2,6	52,5	65,6	15	GaN	H
[18]	5,5	31	30	8,4	SiGe	H
[19]	1,3	35	50	11	GaAs	H
[20]	2,1	47	45	10,5	AlGaN/GaN	M

Table 1: extract of the data base.

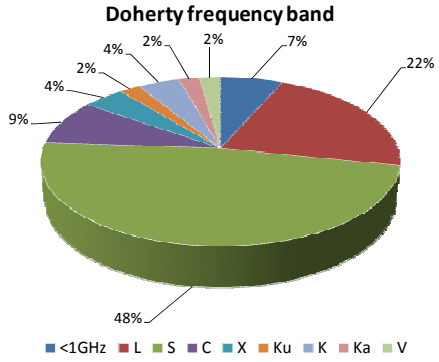

Fig. 4: Frequencies application for DPA.

As it can be noted, almost 50% of DPA realizations are in S-Band (2-4GHz) where the most important wireless systems are located.

Fig. 5 reports the active device technologies used to design DPAs for each frequency bands. As can be observed, in S-band almost the totality of DPAs are realized by using GaN technology and, as will be highlighted later, in a hybrid form. In fact, thanks to the high power capability of GaN devices and the fast prototyping offered by the hybrid structure, it is much more easy to reach high power level together with a simpler circuit layout.

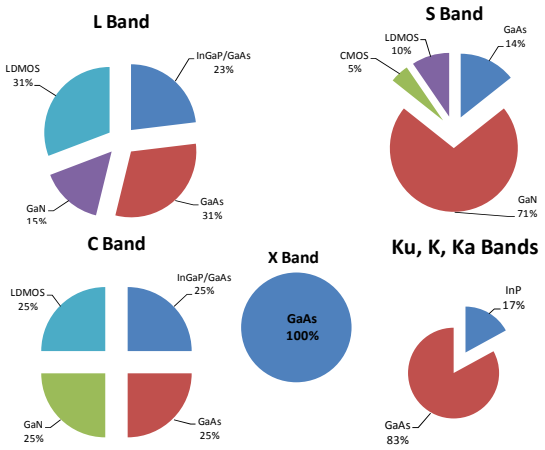

Fig. 5: Active device technologies for DPA.

Fig. 6 shows the output power levels achieved by DPAs realizations as a function of frequency bands, while distinguishing between MMIC and hybrid form. As stated before, the hybrid form is almost always used up to S band, while for upper frequency the MMIC technology is preferred. Moreover, a considerable number of realizations achieved output power levels higher than 50dBm.

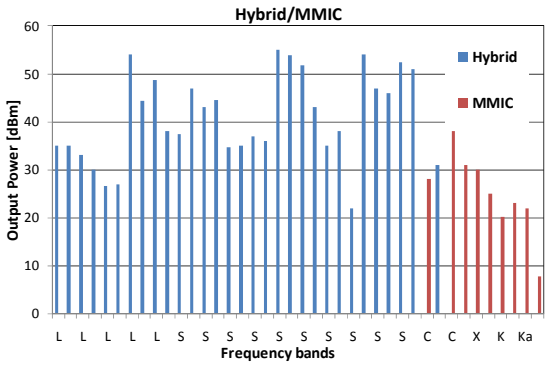

Fig. 6: Hybrid vs. MMIC DPA realizations.

About the key feature of a DPA, Fig. 7 shows the achieved efficiency levels corresponding to both saturation and break point conditions, as a function of frequency bands. It is important to emphasize that the break point represents the power level at which the Auxiliary amplifier is turned on.

Typically, and for all the realizations reported in Fig. 7, the break point is located at 6dB of OBO. As can be noted, with respect to a traditional single ended PA, the DPA architecture assures high efficiency also in back-off, that is a fundamental characteristic for systems that deal with time varying envelope signals.

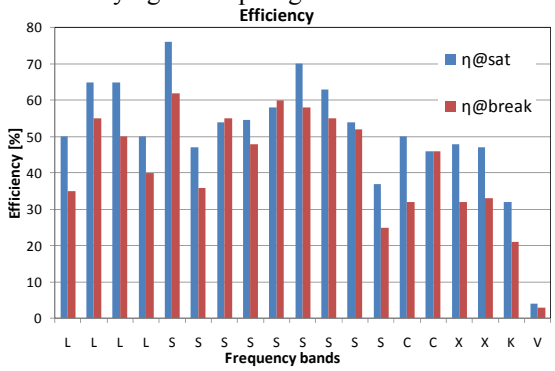

Fig. 7: Efficiency levels of DPA realizations.

As an example of MMIC DPA, Fig. 8 is reported a photo and the corresponding experimental results of a GaAs MMIC DPA realized for X-Band application.

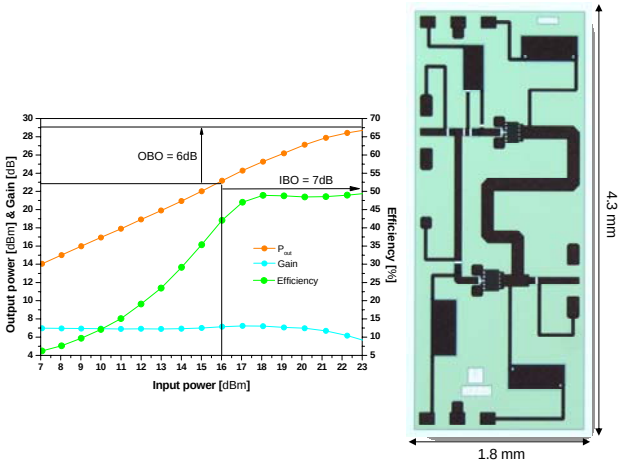

Fig. 8. MMIC DPA for X-Band application.

Analogously, in Fig. 5 are reported the photos of two DPAs for S-Band applications using GaN technology realized in hybrid form. The first DPA has been designed assuring a Tuned Load harmonic configuration for both Main and Auxiliary devices [16]. For the other one, with the aim to further increase the efficiency level achieved by the DPA at the break point, a Class F harmonic configuration has been adopted for the Main device [12]. Regarding the design of the Auxiliary amplifier, also in this case, a TL configuration has still been considered to optimize its performances. In fact, due to the Class C biasing condition, the adoption of other different HT strategies (including the Class F one) would result in a detrimental effect for the Auxiliary device performances [12]. Both are designed by using GaN HEMT (1 mm of gate periphery) as active device to operate at 2.14 GHz, assuring an almost constant efficiency over the usual OBO range of 6 dB.

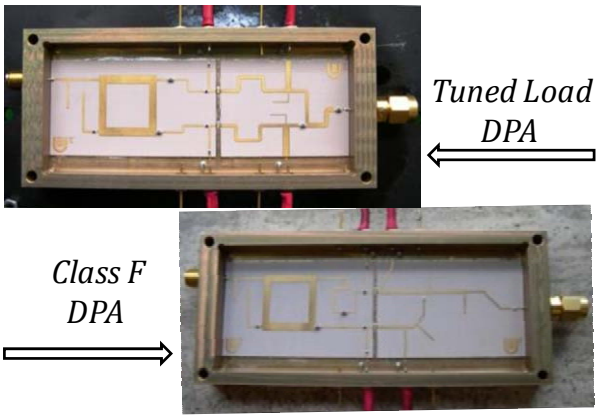

Fig. 9: S-Band hybrid DPAs using GaN technology.

The comparison of the obtained experimental results from the two DPAs is shown in Fig. 10. As can be noted, the expected 15% (roughly) improvement in output power and drain efficiency when using a Class F configuration with respect its TL counterparts has been experimentally demonstrated [12].

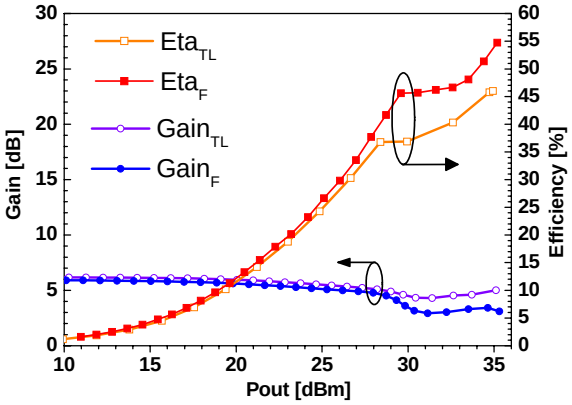

Fig. 10: F-DPA and TL-DPA performances.

On the other hand, one of the main drawback of DPA architecture is related to its intrinsic lower power gain with respect to the nominal value assured by the Main amplifier alone. Fig. 11 shows the gain level achieved by the realizations included in our data base as a function of frequency bands.

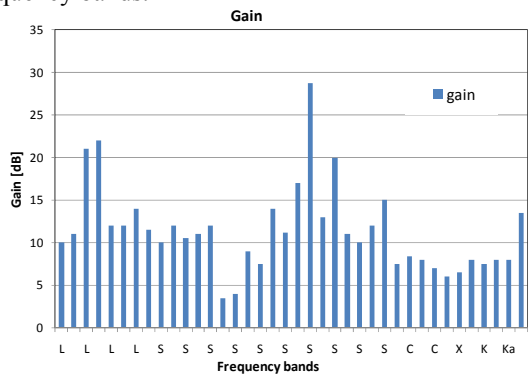

Fig. 11: Gain levels of DPA realizations.

As it can be noted, few realizations have a gain higher than 15dB, despite of the low frequency band and the use of active devices with high available gain levels. Typically, the realizations with higher gain include a driver to increase this feature, with a consequently reduction of the overall efficiency level.

Generally speaking, while comparing the DPA gain with the one achievable through a standard PA, designed by using the same active devices, a drop of about 4-6dB is observed. These fall can be ascribed to both the class C bias condition of the Auxiliary amplifier and the uneven input power splitter. The former is needed to assure the automatic turning on condition at the break point, while the latter is necessary to guarantee the correct dynamic evolution, from the break point to the saturation [21]. In terms of efficiency, this effect could be a problem when, for instance, the DPA has to be integrated in a transmitter chain. In fact, in those cases, a driver stage could be necessary to assure the requested gain level. These driver stages are usually designed to operate as linear system, so their efficiency is typically very low. Therefore, the efficiency of the overall chain is similar to the one of the DPA if and only if its gain is very high. For this reason, in high frequency applications, where the active devices for power applications have usually an available gain lower than 15dB, a gain drop of about 4-6dB for the power stage becomes unacceptable. For practical uses, new ideas to overcome the gain problem are under investigation. For instance, it has been demonstrated that the adoption of different drain bias voltages for the Main and Auxiliary device could be useful to increase the gain of the overall DPA [7]. In this case, to demonstrate the reliability of the proposed design methodology, two different DPAs have been designed, one with the same bias voltages for Main and Auxiliary devices (DPA_1), while the second one (DPA_2) by using different drain bias voltages according to the guidelines derived in [7]. For the design a LDMOS device provided by Freescale Semiconductor has been used, and the operating frequency of 2.14 GHz has been assumed. Fig. 12 shown the comparison between the performance obtained from both prototypes. As can be noted from, both DPAs reach the same saturated output power level (43 dBm), with a quite similar efficiency behavior. However, from Fig. 12 it can be noted that an increase of roughly 2dB in power gain has been obtained with DPA_2. For both DPAs the efficiency is higher than 40% in an OBO of 6dB.

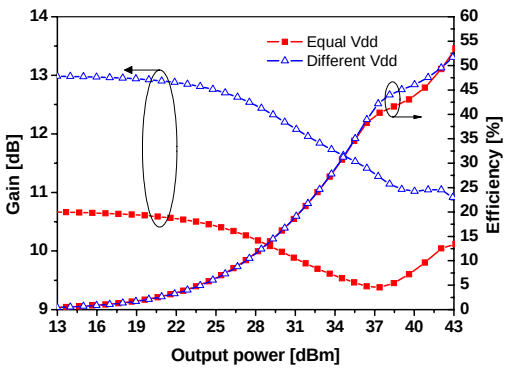

Fig. 12: F-DPA and TL-DPA performances.

Another drawback of standard DPA architecture becomes evident when the PAPR of the signal to be amplified is larger than 8-9dB. In fact, referring to Fig. 13 where the efficiency behaviors of DPAs with different OBO are plotted, in the case of OBO=12dB, the achievable average efficiency is dramatically reduced. Therefore, new solutions to overcome this further drawback are also under study, as the Multi-Stage or N-Stage, sometimes also named Multi-Way DPA [22].

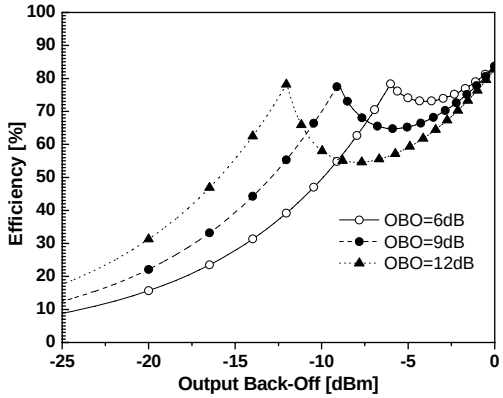

Fig. 13: Efficiency behaviors of DPAs with different OBO.

Finally, looking at the DPA topology, it is possible to note that it is intrinsically based on many narrow bans components, like the IIN, the IPS and the PCN. This aspect restricts the DPA potentialities as best solution for power stage in modern communication systems. In fact, one of the goal of the new systems is to simultaneously operate with more communication standards (i.e UMTS, WiMAX, WiFi ecc.). Since each standard has its frequency band, transmitters with multi-band frequency capability becomes mandatory. Thus, ideas to alleviate such weakness are needed. A possible solution is reported in [8] where the design of a dual-band DPA is demonstrated.

4. CONCLUSION

In this contribution, the evolution of the DPA through its first seventy-five years has been presented. The reasons why this architecture is still on the wave in order to realize power amplifier stages for wireless systems have been highlighted. A review of the DPA principle of operation together with a benchmark of *state of the art* realization methods and fields of application has been reported.

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ANALYSIS OF THERMAL DISSIPATION FOR MM-WAVE FREQUENCY MULTIPLIERS USING GaAs SCHOTTKY DIODES

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ABSTRACT

This paper presents the thermal analysis of a recently realized frequency multiplier for mm-Wave frequencies. The investigation concentrates on a frequency tripler from 110 GHz to 332 GHz. Even though the measurement results show a power handling capability of several tens of milliwatts, for high-power applications, new approaches are needed for effective heat dissipation in the diode structure. The thermal analysis in this work implies a comparative efficiency estimation of two different heat dissipation approaches by means of thermal simulations.

1. INTRODUCTION

Over the years, continual advances of the Schottky barrier diodes into the THz range appear to be most promising for building conventional solid-states sources. The common way to generate power at sub-mm frequencies is by frequency multiplication. Local oscillators could be mentioned as a widely used application of frequency multipliers in heterodyne receiver systems up 1.7 THz [1], [2].

Sub-mm frequency multipliers using Schottky diodes unfortunately show rather low efficiencies. For achieving good performance at these frequencies, the frequency multipliers are hardly pumped with input power. In high powered multipliers there is an additional problem, namely dissipating the waste heat of the input pump power which is not converted into output frequency. For stacked multiplier diodes this is a particular problem, as the middle diodes are located on isolated, poorly-thermally coupled pads and can heat-up to destructive temperatures.

2. 332 GHz FREQUENCY TRIPLER

The frequency tripler uses GaAs Schottky Diodes fabricated at ACST by the so-called Film-Diode process [2]. In contrast to traditional planar structures, Film-Diode fabrication requires two-side processing of the semiconductor wafer, which implies a more complex fabrication, but is more flexible concerning the reduction of structure parasitic and opportunity for an improved thermal dissipation.

The integrated circuit for 332 GHz tripler is shown in Fig.1. It implies two Schottky diodes per arm and is based on balanced configuration. All four diodes with coupling, matching elements and beam-leads are integrated on transferred membrane substrate. The DC-bias beam-line is separated from RF-short by an integrated MIM capacitor. The circuit is designed for the suspended substrate approach waveguide block for achieving optimal performance concerning structure parasitic and RF-losses.

The RF characterization demonstrated good conversion efficiency of about 10% for an input power of about 30 mW. Higher input power led to a total failure of the multiplier.

Due to a particular ACST guard-ring process, the used varactor diodes have an extremely high breakdown voltage which is close to the theoretical limit and is about 15V. EM simulation results suggest that breakdown voltage does not limit the power handling capability. The limiting factor is rather the poor thermal dissipation from middle diodes, which have no direct thermal connection to the waveguide block for a proper heat sink. This is confirmed also by thermal simulations, which suggest a temperature increase up to 450K for the middle diodes for a dissipated power of just 7,5mW per anode. This temperature is beyond the critical temperature for normal operation of Schottky diodes, which is considered about 425K (150°C).

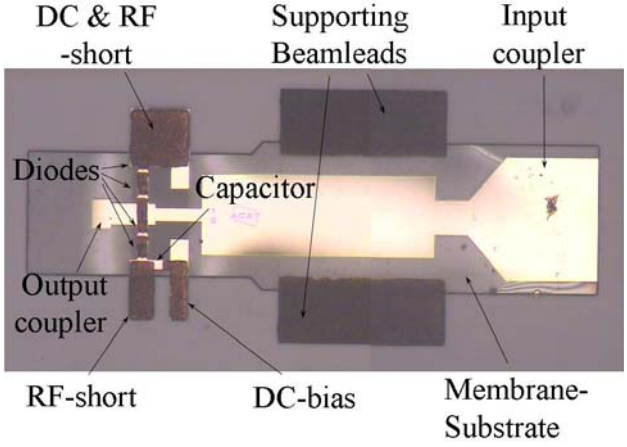

Fig.1: Photograph of the fabricated 332 GHz tripler circuit

3. HEAT SPREADING APPROACHES

Two approaches have been considered for simulations in this work in order to overcome this limitation and to improve the power handling capability of the tripler IC. One approach is to glue a separately fabricated heat spreader of a thermally conductive material, while another one is using an integrated GaAs substrate.

The first approach to dissipate the excessive heat in the anode region is using a thin Chemical Vapor Deposition grown diamond substrate, which shows excellent microwave properties and is the best thermal conductor

known. The diamond pieces may individually be mounted to the membrane device using a particular glue.
The use of a diamond heat spreader suggests good heat dissipation from the anode. Unfortunately there is no glue with good thermal properties suitable for microwave applications. Therefore, the reproducibility of the thickness of the glue-spacing between Au-Pad and diamond may become a concern when series production is considered.
An easier, simpler but nonetheless effective solution is to leave heat-spreader sections of GaAs in specific areas around the anodes, as GaAs itself has reasonable thermal properties (46W/m*K). The big advantage of GaAs over diamond is that the heat sink material now has a perfect thermal contact to the heat-producing area of the varactors and can be guaranteed to be reproducible. There is also no additional handling of the device after processing the wafer, so the risk of accidental damage, like small cracks may greatly be reduced.

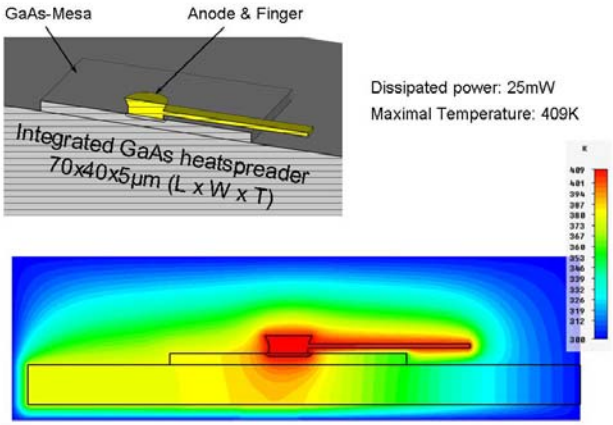

Fig. 2: Thermal analysis of a GaAs heat spreader.

The simulation results reveal the effectiveness of the underlying GaAs forming a heat-sink, as shown in Fig. 2. The maximum temperature occurs in the lower depletion region due to the lower thermal conductivity of GaAs compared to thermal conductivity of Au-Finger contacting the depletion region (anode) from the top. However, the finger structure cannot provide significant contribution to the overall thermal performance of the Schottky diode due to its thin geometry.
The efficiency of the two heat-dissipation approaches was evaluated by comparison. A heat-flow of 75mW per anode was used and the Figure-of-Merit was the maximal temperature in the structure. A temperature above 425K is considered critical for diode operation and can lead to total device failure. The results are shown in Fig. 3. The maximal temperature is drawn versus thickness of the SU-8-spacing and versus thickness of GaAs heat spreader for the first and second approach, respectively. For comparison similar structure without any heat spreader with 75mW of dissipated power per anode leads to temperature increase up to 1780K.
The diamond heat spreader allows very effective heat spreading but thickness of SU8-spacing is very critical. Even a thin SU-8 spacing strongly inhibits the thermal dissipation from the diode and equalizes efficiencies of the two approaches.

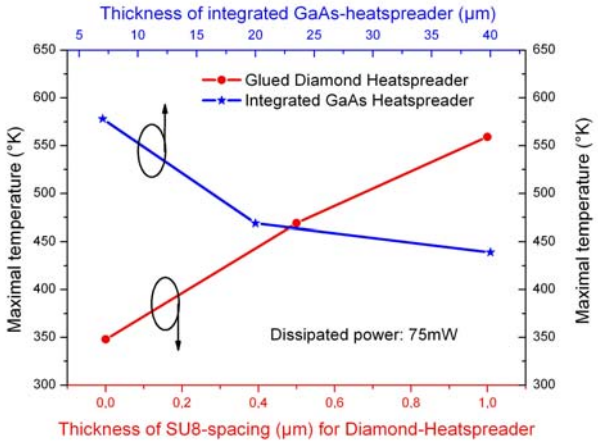

Fig.3: Thermal simulation results of two heat-dissipation approaches

In turn, the second approach appears simpler and more reliable than the diamond. GaAs heat spreaders appear a good alternative to diamond heat spreaders for moderate powers in range of 25mW per anode. Thermal simulations suggest a maximum temperature increase in this case to about 409K.

4. CONCLUSION

Power handling capability of ACST integrated circuit for 332 GHz tripler can be improved by realizing particular heat spreading approaches. Two of such approaches are considered in this work by thermal simulations and results are evaluated in terms of efficiency of thermal dissipation and reproducibility of the fabrication process.

ACKNOWLEDGEMENT

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ADVANCED PHEMT GAAS E/D TECHNOLOGY, MODELING AND CHARACTERISATION

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ABSTRACT

An advanced pHEMT GaAs Enhahcement/Depletion technology is presented in this paper. The fabrication process involves a specific approach based on a double etch epi-structure in order to obtain depletion and enhancement mode pHEMT on the same wafer.
We report the development status of the GaAs E/D technology through the analysis of DC and RF characterization. Based on the analysis and discussion of some figure of merits and device's parameters, the technological process advancement is investigated. Finally, devices modeling activity results are described.

1. INTRODUCTION

Modern electronic systems for emerging applications require high performance active device development in order to ensure higher functionality and design flexibility. The wafer-level integration of GaAs Enhancement-mode with Depletion-mode pHEMT is becoming a very appealing technology since it offers a number of significant advantages over conventional III-V technologies. The most important feature relies in the possibility of monolithic integration of both RF analog (switches, low noise amplifiers, power amplifiers), application field where GaAs offer superior performance than the Si counterpart, and digital functionalities (logic controls - typically performed by a separate Si CMOS-based die) on the same GaAs chip in conjunction with compact die size and weight as well as low manufacturing costs. During the last years, interest in such solution is growing thanks to specific applications e.g. phased array antennas for civil and military applications, commercial mobile smart antenna market and satellite equipment. Therefore there is a need for the development of technologies which can support both operations in a multi-functional environment.
For a long time, the development of GaAs-based digital ICs has been hindered by the lack of compatible integration process for both D-mode and E-mode HEMTs. Due to lack of p-channel GaAs based HEMTs, a circuit configuration like CMOS cannot be implemented yet. Using n-channel HEMTs, direct-coupled FET logic (DCFL), which features integrated E/D-mode HEMTs technology, offers the simplest pHEMT-based digital circuit configuration [1,2]. The main disadvantage of DCFL is its low noise margin, which is sensitive to threshold voltage variation. Therefore, for a E/D technology to be usable its mandatory to accurately control the threshold voltage. Moreover, it's important that devices exhibit low defect density in the device's channel region and as low as possible ON-state resistance in order to get the best possible dynamic performance.

2. DEVICE STUCTURE AND TECHNOLOGY

In order to achieve the above mentioned device properties, a double stop etch epi-structure was developed. The devices structure is depicted in Fig. 1.

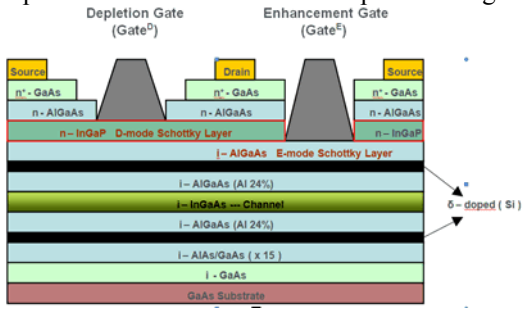

Fig. 1: Device structure section view.

A first n-InGaP etch stop layer is introduced to obtain a Depletion-mode devices by etching selectively n+-GaAs and n-AlGaAs layers. To acquire on the same substrate an Enhancement-mode pHEMT, we have set up an i-AlGaAs second etch stop layer where 0.4 µm Gate contact is realized after selectively removing of n-InGaP layer.

3. EXPERIMENTAL RESULTS

3.1. DC and RF characterization

DC characterization was performed on standard analog pHEMT and on small Gate periphery pHEMT for digital circuit applications. The DC transfer characteristics of 4x50 µm E/D pHEMT are show in. Analyzing the depicted curves, good pinch-off characteristics are observable for both D- and E-mode device and this also put in evidence a good 2DEG channel confinement. The Drain current densities are comparable for both device types and equal 180 mA/mm and 220 mA/mm with a high peak transconductance of 415 mS/mm and 450 mS/mm for E and D-mode devices respectively. Results

that are well comparable to other available commercial E/D technology [3].

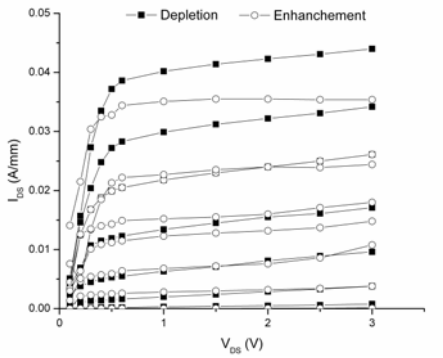

Fig. 2: Normalized drain current characteristics for D-mode (square) and for E-mode (circle) 4x50 µm pHEMT.

Mean measured devices' threshold voltages of small peripheries (2x2, 2x4 2x10 µm) digital D-mode pHEMT is -0.6 V on wafer yield of 90 % and for E-mode type is 0.23 V on wafer yield of 75%. Such threshold voltage differences between E and D mode pHEMT is remarkable and mitigate also the observed parameter spread in E mode devices. The evaluated specific ON-resistance was equal to 1.8 Ω/mm and 1.9 Ω/mm for D and E-mode pHEMT respectively. About Gate leakage current on E-mode device, we observed a junction forward conduction starting from $V_{GS} \geq 0.8$ V thus limiting device's performance and usability above that limit.

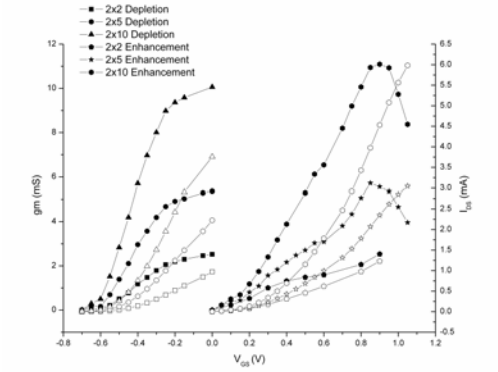

Fig. 3: Drain current (hollow symbol) and transconductance (filled symbol) of D and E-mode pHEMT of different device size.

High frequency characterization was carried out by means of on-wafer microwave S-parameter measurement. Using coplanar wafer probe, on-wafer measurement up to 40.1 GHz was accomplished. The values of f_T are higher than 30 GHz and 35 GHz for the D-mode pHEMTs and the E-mode pHEMTs respectively and the corresponding f_{max} values are higher than 40 GHz in both cases. RF measurement was carried also on common-gate transistor that acts as a FET-Switch device that was on the same wafer.

3.2. Device modeling

Equivalent circuit model for both analog and digital pHEMT was extracted. Small-signal multi-bias equivalent circuit representation was achieved for analog E/D pHEMT based on a well-established topology and procedure [4, 5]. Common gate pHEMT measurement was devoted to characterize the insertion loss and return loss of different size device in terms of numbers of finger (N) and channel width (W). Based on those measurement, a simplified model valid up to high frequency was evaluated. The models describe in a simplified manner the behavior of the transistors in two different Gate biasing condition, i.e. strong channel pinch-off (OFF state) and open channel (ON state, see Fig. 4).

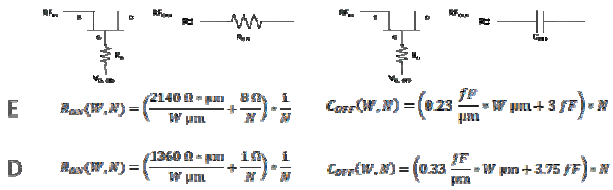

Fig. 4: simplified FET-Switch models and scaling rules.

Due to the simplification introduced formulating the FET-Switch model, the scaling rules law are valid for N < 8 and for W ≤ 150 µm only.
Finally, digital pHEMT non-linear model was evaluated. The DC drain current was modeled on the bases of Chalmers Angelov model [6] tailored for digital circuit design.

4. CONCLUSIONS

In this work, GaAs E/D pHEMT technology was investigated. From the investigation of all experimental data the development of GaAs E/D pHEMT technology seems to need only little refinement form the point of view we considered so that other technological investigation about other device properties and aspects, like reliability, starts. The double etching process approach gives to devices good DC and RF performance suggesting this approach as a valuable one to implement E/D mode pHEMT on the same wafer.

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C-BAND MMIC CHIPSET AND DIGITAL CONTROL CIRCUITS FOR T/R MODULES BASED ON GaAs ENHANCEMENT/DEPLETION TECHNOLOGY

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ABSTRACT

A GaAs Enhancement/Depletion process represents the enabling technology to fabricate mixed-signal circuits for microwave applications onto the same chip, thus making it suitable for MMIC-based T/R Modules. A GaAs E/D process technology has been developed to this goal: analog and digital test vehicles are addressed to demonstrate process potentials. In this contribution, a 6-bit Phase Shifter, a 5-bit Attenuator and a Buffer Amplifier operating at C-Band are presented. Besides, simple digital circuits and a more complex 8-bit Serial-to-Parallel Converter are illustrated to demonstrate digital functionalities integrated over a GaAs substrate.

1. INTRODUCTION

In recent years many solutions have been investigated to bring T/R modules in a fully integrated form with additional signal conditioning (phase and attenuation) and on-board digital controls [1-4]. The reason of this trend is correlated to the use of multi-functional chips in phased array antennas, where a high number of multi-function modules are needed. A technological process, capable of providing small FET devices for digital operation and standard FET devices for RF analog operation, both in normally-on or normally-off mode, is well-suited for monolithic realization of such mixed-signal circuits.
This contribution describes a technological process based on a double stop etch epi-structure that allows both Enhancement and Depletion mode device fabrication onto the same chip. Then MMIC Attenuator, Phase Shifter, Buffer Amplifier and a Serial-to-Parallel Converter designs are illustrated to demonstrate process capabilities and multi-function integration.

2. E/D TECHNOLOGICAL PROCESS

The capability to fabricate very small digital devices together with RF transistors leads to the integration of usual RF signal conditioning functions with on-board digital controls.
In order to achieve this goal, a 0.4 µm GaAs pHEMT technological process has been developed, based on a double stop etch epi-structure, as shown in Fig. 1. An heavily doped cap GaAs layer is utilized to form

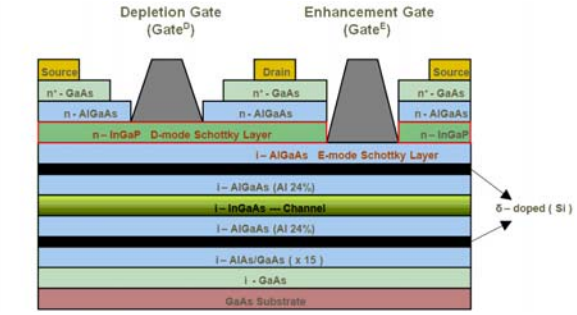

Fig. 1: E/D device process cross section

Au/Ge/Ni low resistivity ohmic contact. A first n-InGaP etch stop layer is introduced to obtain Depletion Mode devices by etching selectively n+-GaAs and n-AlGaAs layers. To acquire on the same substrate an Enhancement mode PHEMT, that exhibits a normally fully depleted channel, an i-AlGaAs second etch stop layer has been implemented, where the Gate contact is positioned after selectively removing the n-InGaP layer.

3. MMIC CHIPSET DESIGN

MMIC Test vehicles operating at C-Band (5.1–5.9 GHz), implementing the typical RF signal conditioning functions, are presented. The chipset consists of a 5-bit Attenuator, a 6-bit Phase Shifter and a Buffer Amplifier.

3.1. 5-bit Attenuator

The 5-bit Attenuator features 1 dB step resolution and up to 31 dB attenuation dynamics. Each bit is based on the Bridged-T circuit topology and the differential attenuation is achieved by means of two cold D-FETs with complementary control bias. An additional capacitor on the shunt arm minimizes the insertion phase difference between the reference and the attenuation states [5]. Attenuator's expected performance over the

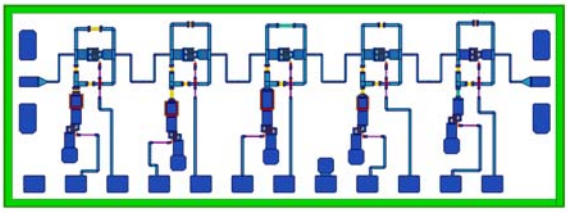

Fig. 2: Layout of the 5-bit Attenuator

5.1-5.9 GHz bandwidth are listed in Table 1. The corresponding layout is shown in Fig. 2. Chip size is 4.3x1.5 mm^2.

3.2. 6-bit Phase Shifter

The 6-bit Phase Shifter features 360° phase shift range with 5.625° phase resolution. Bits from 5.625° to 45° are designed according to the reconfigurable All-Pass filter topology [6], while 90° and 180° cells are based on Switched HI-Pass/LO-Pass topology [7]. Cold D-FETs enable switching between reference and phase shifted states. Table 1 illustrates the Phase Shifter expected performance over the operating bandwidth, while the corresponding layout is shown in Fig. 3. Resulting die size is 4.3x3.7 mm^2.

3.3. Buffer Amplifier

The Buffer Amplifier consists in a compact single-stage amplifier (0.7x1.0 mm^2), aimed at separating a phase conditioning cell from an amplitude conditioning one and viceversa, in order to minimize interactions between these two functionalities. The amplifier expected performance over the operating bandwidth is summarized in Table 1.

Function	Figure of Merit	Value
Attenuator	RMS error (dB)	< 0.36
	Spurious RMS error (deg)	< 3.7
	IRL, ORL (dB)	> 19
Phase Shifter	RMS error (deg)	< 5
	Spurious RMS error (dB)	< 1.4
	IRL, ORL (dB)	> 10
Buffer	Insertion Gain (dB)	> 12
	IRL, ORL (dB)	> 11

Table 1: MMIC Chipset's expected performance.

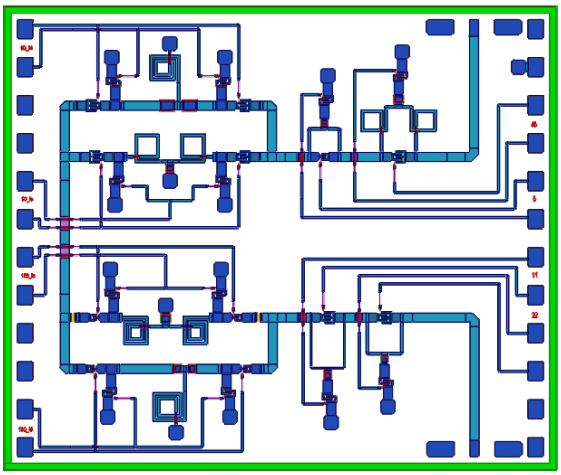

Fig. 3: Layout of the 6-bit Phase Shifter.

4. DIGITAL CIRCUITS DESIGN

The digital circuits design is based on Super Buffered FET Logic (SBFL) [8, 9]. For its effective implementation, an E/D technology is necessary since both Enhancement and Depletion mode devices are required. Simple test cells like NOR ports and D-Flip Flop were designed as building blocks of a more complex 8-bit Serial-to-Parallel Converter, whose layout is shown in Fig. 4.

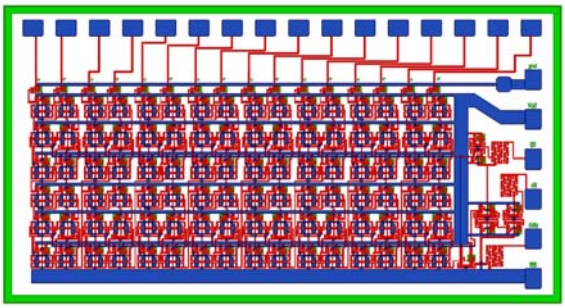

Fig. 4: Layout of the Serial-to-Parallel Converter

It consists in a 8-bit Shift and 8-bit Hold Registers. Inputs feature TTL interface by means of Input Level Shifters. Output control voltages are between 0 V and -3.8 V, that are the ON and OFF bias voltages for Depletion devices operating in switching mode. Chip size is 4.2x2.2 mm^2.

5. CONCLUSION

In this paper, the signal conditioning blocks typically implemented in T/R Modules were presented and designed in GaAs E/D MMIC technology. In fact, to allow the integration of RF circuitry with digital controls, it is mandatory to fabricate normally-on and normally-off devices within the same technology. To this goal, a technological process, based on a double stop etch epi-structure, was successfully developed. Although this technology is in its early development stage, MMICs expected performance exhibits promising values and prefigure their utilization in phased array systems.

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HIGH LEVEL OF AUTOMATED PROCESS FOR BROADBAND AND X-BAND MMIC'S PRODUCTION

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ABSTRACT

In this paper we propose an advanced fully automated high yield process to fabricate MMIC based on 0.25 µm T-gate technology. The industrialization of such process will make available a mature technology suitable to satisfy the increasing demand for military and space wide-band and X band T/R modules applications. RF Device performances have been evaluated focusing our attention to Power Amplifier (PA) and robust Low Noise Amplifier (LNA).

1. INTRODUCTION

Phased-array radar systems, based on active electronically scanned antennas (AESA) populated with a high number of Transmit/Receive (T/R) modules, are on the cutting edge of advanced radar technology and in the near future will dominate in all application domains (terrestrial, naval, avionic and space). Furthermore, since modern defense platforms call for multi-function/multi-domain RF systems with radar, EW and communications capabilities, AESA systems are in charge of operating over multi-octave bandwidths. This kind of systems will have to cover C and X band to execute radar functions, but will also have to guarantee coverage up to Ku band to perform Electronic Warfare tasks (i.e. ECM, ESM) and Communication.

2. MAIN TECHNOLOGICAL STEPS

2.1. Advanced epilayer structure

A proper epilayer structure should be designed to develop an optimized PHEMT for high frequency high power applications. In particular to obtain a high breakdown voltage and high transconductance PHEMT physical device simulation has performed in order to optimize the structure in terms of layer sequence, layer thickness, doping levels and chemical composition. To further improve device breakdown a suitable gate recess geometry, i.e. double recess profile, is introduced to manage high electric field in the gate region. A double recess geometry requires a first recess step to remove the n^+-GaAs cap layer and then a second wet etch to reach the AlGaAs Schottky layer. In order to simplify the gate recess fabrication procedure, allowing an automation in the process, an advanced epilayer structure, including two stop etch layer, have been introduced [1].

2.2. Gate contact optimization

The main challenge in fabricating high frequency high performance device is related to define proper gate profile capable to reduce gate length, i.e. gate capacitance, avoiding any increase in gate resistance that could be detrimental for final RF performances.

A T-shape gate geometry represents the standard solution to said requests, although to develop this T-shape an high control process, in terms of gate lithography, wet chemical process, metal layer evaporation is mandatory.

The common technique to fabricate sub-half-micron structures make use of e-beam lithography process by which is possible to define suitable resists profiles for complex T-shaped structures. In particular we have optimized a resist profile compatible to the subsequent wet chemical etch and final evaporation process. As a result of our process optimization we are able to obtain gate contact resistance comparable to our standard 0.5µm gate length device (Fig. 1).

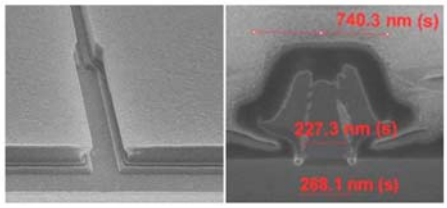

Fig. 1: Left: E-beam resist profile utilized for T-gate formation; Right: FIB section of the T-gate contact

3. DEVICE RF PERFORMANCES

An extensive measurements campaign has been performed on 0.25µm PHEMT to evaluate RF performance. As a test vehicle a 10x100µm FET (namely A10D) has been fully characterised on all processed wafers. Such Device Under Test (DUT) is actually the reference to design and to fabricate different MMICs prototype as far 6-18GHz and 4.5-18GHz HPAs. The same technology has been evaluated also for low-noise

applications using 4x75µm FET as a DUT.

3.1. Power performances

In order to investigate the linear RF performance, some commonly used Figures of Merits (FOMs) as Maximum Available Gain (G_{Max}), Short Circuit Gain (H21), Maximum oscillating frequency (f_{Max}) and cut-off frequency (f_T) have been estimated. In particular G_{Max} and H_{21} behaviour vs frequency are reported in Fig. 2 for minimum, medium and maximum statistical device. We have measured circa 16.5dB@10GHz and f_{Max} 70 GHz while from the H21 graph we can extrapolate an f_T of circa 27 GHz with quite small dispersion as indication of high wafer uniformity (Fig. 2, left).

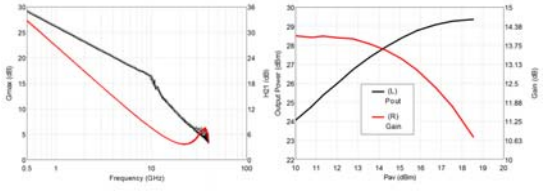

Fig. 2 Left: Linear Gain Performances: Gmax (black lines, black solid line is the medium A10D) and H21 (red lines, red solid line is the medium A10D) behavior vs. frequency @ V_{DS}=8V I_{DS}=30%I_{DSS}, in CW mode; Right: Power performances @ V_{DS}=8V, I_{DS}=30%I_{DSS}, @ 10GHz in pulsed condition with T_{ON}=100µs and Duty=10%.

To evaluate output power performances, a source/load-pull campaign has been performed on medium A10D device. Such measurements have been performed in pulsed condition through pulse duration of 100µs and a 10% Duty Cycle. The nonlinear characterization has been performed at 10GHz with a pulsed Drain Bias of 8V and I_{DS} of 30% I_{DSS}. Load Pulls have been performed at 3dBc to identify the output optimum load maximizing the output power. On said condition Power sweep P_{out} vs P_{IN} is shown in Fig. 2, right. We have measured a power density of circa 0.9 W/mm @ 3dBc and G_{ASS}(3dBc) ≈ 11 dB.

3.2. Robust Low-Noise Performances

To evaluate the robustness of this technology for LNA application we have performed stress tests on 4x75µm FET at 2.5V and 25% I_{DSS}. The stress tests procedure is to expose biased FET to a calibrated input RF power (@10 GHz) for 10 second and after this stress measuring the transistor Gain and Drain/Gate current. Such process was repeated by increasing the input RF drive level, as depicted in Fig. 3. As shown, small signal gain starts to degrade close to 30dBm that represent also input power for which the device is destroyed. Gate leakage remains practically unchanged and less then 0.02 mA/mm. Regarding noise performance we have measured @ 10 GHz for this 4x75µm FET circa 1 dB minimum noise figure.

4. HPA PROTOTYPE PERFORMANCES

In order to evaluate the process capability we have developed different HPA prototypes for different application band. In particular we have fabricated Wide Band HPA (4.5-18 GHz and 6-18 GHz), and Narrow Band C-Band and X-Band HPA. (see Fig. 5).

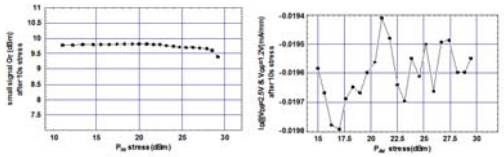

Fig. 3: Signal gain and gate leakage after stress for a 4x75µm test FET

Wide Band HPAs have a total gate periphery of 7 mm, a chip size of 5.2x2.9mm and an RF on-wafer yield greater than 85%. For the 4.5-18GHz HPA, an Output Power of 33±1dBm, PAE 25 ± 5% and a Linear Gain greater than 16dB have been measured in the whole frequency range.

For the 6-18GHz HPA, an Output Power of 34±1dBm, PAE 24±4% and a Linear Gain greater than 17dB have been measured in the whole frequency range.

Narrow Band HPAs in C and X-Band have a total gate periphery of 24mm and 26.4mm, a chip size of 3.8x4.0mm and 3.8x4.2mm, a yield greater than 77% and 75% respectively. For the C-Band HPA, an Output Power of 40.5±0.5dBm, PAE 38±2% and a Linear Gain greater than 19.5dB have been measured. For the X-Band HPA, an Output Power of 40.8±0.5dBm, PAE 35±2% and a Linear Gain greater than 18dB have been measured.

The above results show an evident and well known correlation between on-wafer yield and total gate periphery, in any case greater than 75%. This remark is particularly relevant if we consider that in case of X-Band HPA we have 26.4mm total gate periphery confirming the reliability of our process.

5. CONCLUSIONS

We have developed 0.25 µm PHEMT process capable to ensure high performance, high yield MMICs fabrication. Our proprietary technology is compatible to a complete automated process and therefore reduces time and process cost. In the first prototype evaluation we have demonstrated excellent results for all the frequency bands that are of primary interest for the next generation of phased-array radar systems.

ACKNOWLEDGMENT

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ANISOTROPIC TRANSPORT OF InAs/AlSb HETEROSTRUCTURES GROWN ON InP SUBSTRATES

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ABSTRACT

Anisotropic behavior of the InAs/AlSb epitaxial structure is presented. DC measurements show anisotropy of the sheet resistance, of the mobility and of the HEMT figures of merit g_m and $I_{DS,max}$. Furthermore, it has been found that the anisotropy is even enhanced at cryogenic temperatures. The anisotropic transport behavior of the InAs/AlSb heterostructure has been related to the presence of threading dislocations in the strained AlSb metamorphic buffer.

1. INTRODUCTION

The high electron peak velocity, the large conduction band offset and the high electron concentration in the InAs channel, combined with the small bandgap of the InAs (0.36 eV), make the AlSb/InAs high electron mobility transistor (HEMT) a promising device candidate for high frequency and ultra low power applications [1], [2]. However, the large lattice mismatch between the InP substrate and the InAs channel, leads to a challenging growth of the heterostructure. Therefore, the use of the AlSb metamorphic buffer is needed to accommodate the large tensile strain in the InAs channel [3]. We here report on the anisotropic transport in the 2DEG, for the AlSb/InAs HEMT grown on InP substrate.

2. STRUCTURE CHARACTERIZATION

The surface morphology of the AlSb/InAs HEMT has been first characterized through the use of atomic force microscopy (AFM). The complete epitaxial structure is shown in Fig. 1. In Fig. 2, it is shown the AFM scan of the top surface of the heterostructure, where it is possible to observe the presence of elongated features oriented in the [1$\underline{1}$0] direction. The cause of these features has then been further studied by scanning transmission electron microscope (STEM) analysis. In Fig. 3, the STEM picture of the AlSb/InAs HEMT structure is shown, revealing the presence of threading dislocations starting in the strained AlSb metamorphic buffer and propagating throughout the structure up to the InAs channel. This result in a not uniform growth of the InAs channel, and then of the subsequent layers, which leads to an oriented crack as also seen in the AFM analysis.

InAs:Si doped	50 Å
$In_{50}Al_{50}As$	40 Å
AlSb	80 Å
Te δ-doping	$4x10^{12}$ cm^{-2}
AlSb	50 Å
InAs Channel	150 Å
AlSb	500 Å
$Al_{80}Ga_{20}Sb$	2500 Å
AlSb	7000 Å
$In_{50}Al_{50}As$	1000 Å
S.I. InP Substrate	

Fig. 1: AlSb/InAs HEMT epitaxial structure.

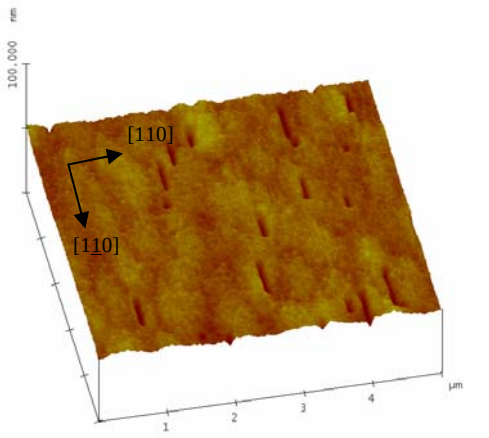

Fig. 2: AFM measurement of the AlSb/InAs HEMT surface.

2. ELECTRICAL CHARACTERIZATION

Electrical characterization has been performed in order to verify the effect on the two dimensional electron gas (2DEG) transport of the elongated cracks in the channel. For this purpose, different types of test structures such as transmission line model (TLM), Hall bar and HEMTs have been fabricated oriented along different directions. The total resistance R_T versus the contact distance d of TLM structures oriented along the [1$\underline{1}$0] direction, parallel to the cracks, exhibit a lower slope, *i.e.* lower

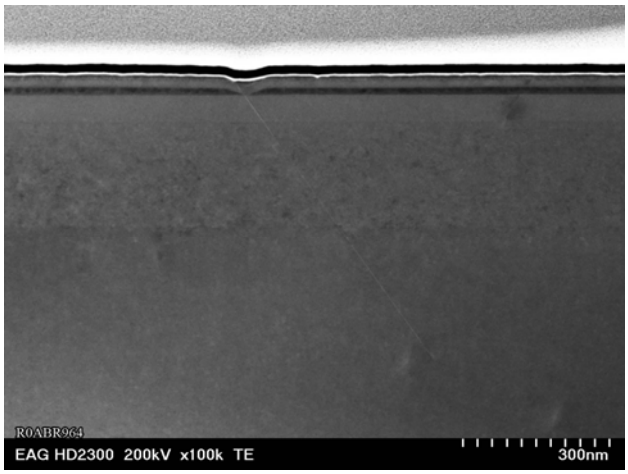

Fig. 3: STEM picture of the InAs/AlSb HEMT structure. The presence of a threading dislocation in the AlSb buffer, leading to a pit in the InAs channel, is clearly visible.

sheet resistance R_{SH}, compared to that of TLM structures oriented along the [110] orthogonal direction; See Fig. 4. R_{SH} is 118 Ω/sq and 174 Ω/sq along the directions [1$\underline{1}$0] and [110] respectively. Furthermore, TLM oriented along the diagonal direction [100] show an intermediate R_{SH} value of 140 Ω/sq.

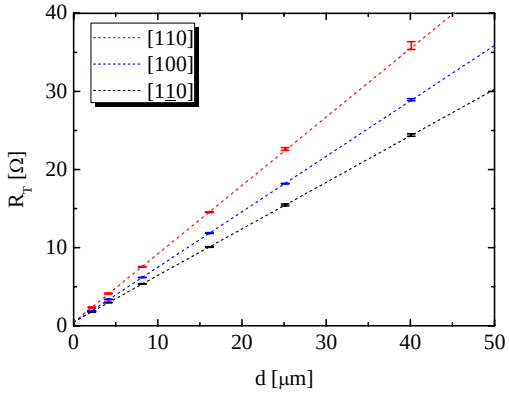

Fig. 4: Total resistance R_T versus contact distance d for TLM structures oriented along three different orientations.

TLM structures have also been measured varying the temperature from 300 K down to 6 K. From the extracted R_{SH} value at each temperature, the mobility μ_n has been calculated using the equation:

$$\mu_n = \frac{1}{q \cdot n_s \cdot R_{SH}} \qquad (1)$$

where the carrier concentration n_s, in the quantum well, is considered constant with temperature. In Fig. 5, μ_n is plotted versus temperature for the two orthogonal directions. It is observed that the anisotropy in the mobility is enhanced when reducing the temperature with a difference, along the two directions, up to 170% at 6 K. HEMTs with the channel oriented along the two orthogonal directions have also been measured. As can be seen in Fig. 6, the HEMT oriented parallel to the [1$\underline{1}$0] direction shows 30% higher g_m and 25% higher $I_{DS,max}$, compared to the one parallel to the [110] direction. The electrical anisotropy measured in TLM and HEMT devices is related to the presence of elongated cracks in the channel [4].

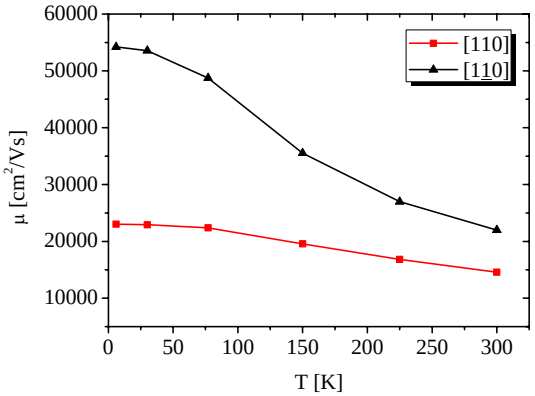

Fig. 5: Calculated μ_n versus T along the two orthogonal directions [1$\underline{1}$0] (triangles) and [110] (squares).

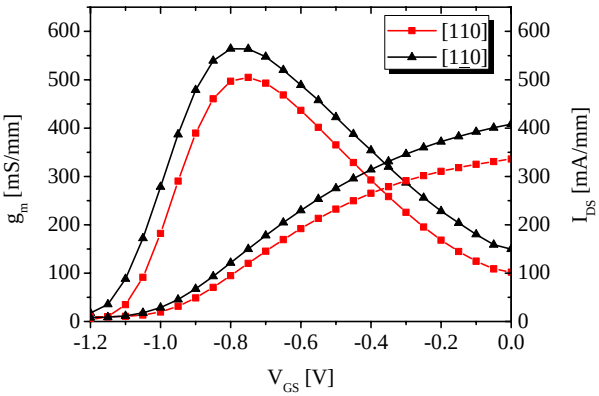

Fig. 6: I_{DS} and g_m versus V_{GS} for HEMTs with the channel oriented along the two orthogonal directions [1$\underline{1}$0] (triangles) and [110] (squares).

4. CONCLUSIONS

Anisotropic transport behavior in the InAs/AlSb heterostructure has been found. TLM structures, showed lower R_{SH} and higher μ_n along the [1$\underline{1}$0] direction. The HEMT devices also showed higher g_m and higher $I_{DS,max}$ along the [1$\underline{1}$0] direction. This anisotropic behavior has been correlated to the presence of elongated cracks in the InAs channel caused by threading dislocations in the AlSb metamorphic buffer.

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SAMPLE-AND-HOLD CIRCUITS USING InAs NANOWIRE FETs

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ABSTRACT

Sample-and-hold (S/H) circuits are designed by using InAs nanowire (NW) FETs. An experimental S/H circuit, consisting of a NW FET, a sampling capacitor, and a simple output buffer, is demonstrated. A novel circuit which can improve the resolution even in the presence of leakage current of InAs NW FETs is also proposed.

1. INTRODUCTION

InAs nanowire (NW) FETs are expected to have a large transconductance (g_m) because of a high electron mobility of InAs and efficient gate controllability on the drain current due to a surrounding gate configuration. This is attractive from a view of ultrahigh-speed sample-and-hold (S/H) circuit applications [1], where a high drain-current drivability is essential to charge/discharge a sampling capacitor under very high sampling frequencies. Since this is difficult to achieve by using a conventional CMOS technology, the S/H circuit is one of the most promising candidates of NW FET applications. Once the high-speed signal is captured by the S/H circuit, CMOS circuitry is capable to process the signal in the digital domain with parallel signal-processing architecture.

2. FABRICATION AND CHARACTERIZATION OF SIMPLE S/H CIRCUIT

Fig. 1 shows the schematics of a simple S/H circuit consisting of a switching FET M_1, a capacitor C_h, and an output buffer, where the analog input signal is held as a certain amount of charges when M_1 is turned off. The transistor M_1 shall be an InAs NW FET. The InAs NWs were synthesized in a metal-organic vapor phase epitaxy system using the vapor-liquid-solid (VLS) growth mode. Colloidal Au nanoparticles of 50 nm diameter were used as seed elements on GaAs(111) growth substrate. The 12 µm long InAs nanowires were mechanically transferred into isopropyl alcohol. For circuit integration of nanowires control over the position and orientation of nanowires is absolutely necessary. This has been successfully done by field-assisted self-assembly (FASA) [2]. The NW solution was dropped on a semi-insulating InP substrate which contains pre-patterned electrodes of 15 nm Ti in order to assemble the nanowires by FASA deposition [2] at predefined positions.

Fig. 2 shows micrographs of a fabricated circuit. The output buffer consists of two MISHFETs, M_2 and M_3, which were integrated with the NW FET by using a conventional InP-based process.

Fig. 3 shows the input and output waveforms experimentally obtained from the circuit shown in Fig. 2. Although offsets were observed at the transition from the track mode to the hold mode due to the clock feed through, the basic sample-and-hold circuit operation has been confirmed. If a differential scheme would be used, these offsets could be minimized.

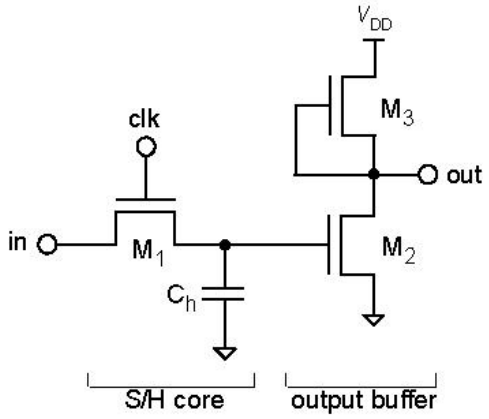

Fig. 1: Sample-and-hold (S/H) circuit configuration.

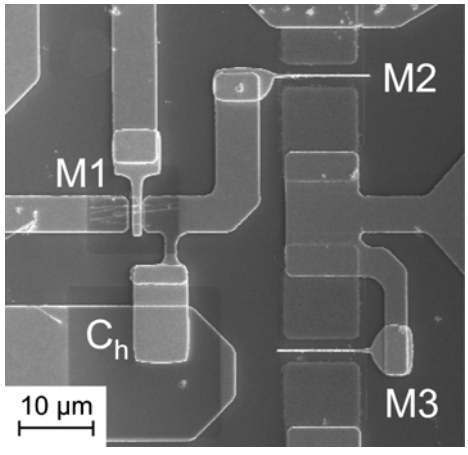

Fig. 2: Fabricated S/H circuit using an InAs nanowire MISFET M1 consisting of six nanowires as a channel and the sampling capacitor C_h. The output buffer is fabricated using InP based HFETs (M2, M3).

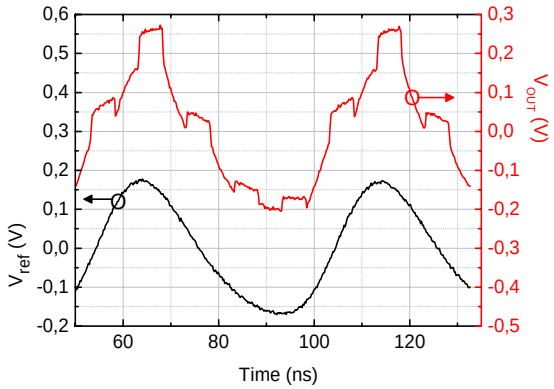

Fig. 3: Input and output waveforms obtained experimentally from the circuit shown in Fig. 2.

3. PROPOSED S/H CIRCUIT

A drawback of a present InAs NW FET is relatively large leakage current in the off-state. The on/off ratio is sometimes around 100. Our circuit simulation reveals that much higher on/off ratios of the drain current are needed to achieve an accurate (or high bit-resolution) sampling in conventional S/H circuits, while a large g_m is necessary to obtain high-speed operation. The leakage current causes signal feed through and droop in the hold mode, which deteriorate the sampling accuracy. Another challenge in designing an S/H circuit with NW FETs is to keep the number of NW FETs used in the circuit as small as possible.

To improve the resolution even for an on/off ratio as low as 50, a novel differential-mode S/H circuit as shown in Fig. 4 is proposed. This includes additional signal paths to cancel the low-frequency leakage current by using M_{15} and M_{16}. These FETs add the complement signals supplied to the opposite polarity input terminals. The amplifiers with a gain of three are also included to effectively suppress the effect of the leak current. M_{13} and M_{14} provide high-frequency-signal cancelation paths by capacitive coupling between the source and drain nodes [3]. The bias voltages V_{b1} and V_{b2} are chosen so that M_{13} to M_{16} are turned off.

Fig. 5 shows the estimated resolution as a function the sampling frequency. A simple S/H circuit results in a low resolution of around 2 bits because the leakage current in the off-state switching FETs causes droop in the hold phase. A modified circuit with the ac signal cancelling paths [3] results in a slight improvement in the resolution. A drastic improvement has been obtained for the present circuit, where the resolution can be improved up to 7 bits. It should be noted that the smaller sampling-capacitance value is beneficial to reduce the charging time, but it results in a large droop in the hold mode. Therefore, there is an optimum capacitance value for each sampling frequency, which varies from 10 pF to 0.1 pF in this simulation as the sampling frequency increases.

The maximum sampling frequency is limited by g_m. In this simulation, 160 μS is assumed for the NW FET, which is based on an experimentally obtained value [4]. If a larger g_m is available by using, for example, shorter gate length switching FETs, the sampling frequency can be faster while keeping the resolution constant.

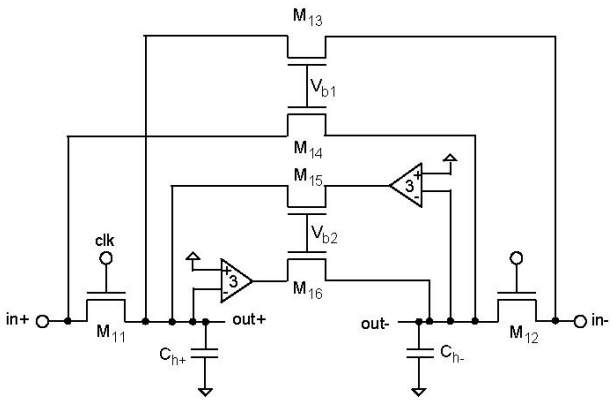

Fig. 4: Proposed S/H circuit to suppress the effect of leakage current on the sampling resolution.

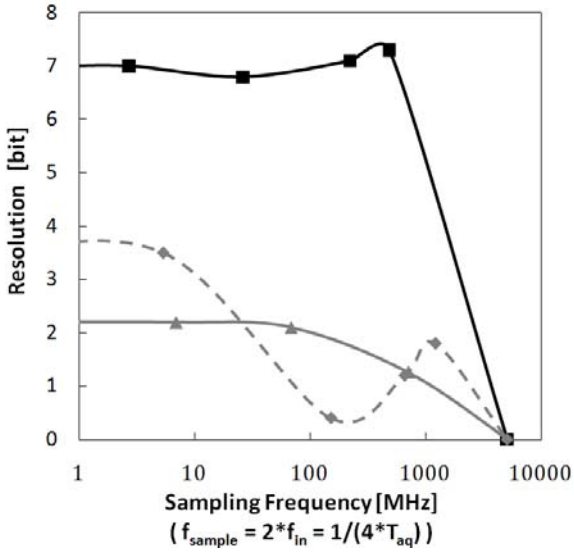

Fig. 5: Estimated resolution as a function of the sampling frequency circuit of Fig. 4 with high-frequency signal cancellation paths [3]: gray triangles w/o M13-M16 transistor, diamonds with M13-M14, black squares with M13-M16.

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FABRICATION AND CHARACTERIZATION OF InGaAs/InAlAs SLOT DIODES

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ABSTRACT

The slot diode is a component similar to a gate-less high-electron mobility transistor (HEMT). The slot diode can potentially act as a tunable terahertz semiconductor generator across a large bandwidth. In this work, we have designed, fabricated and characterized slot diodes. The starting material was a single δ-doped InGaAs/InAlAs HEMT-structure on an InP bulk substrate. A standard InP HEMT process was used for the slot diode fabrication. DC measurements of the output current revealed the presence of a kink for V_{DS} = 0.5 V.

1. INTRODUCTION

InGaAs/InAlAs planar slot diodes have been predicted by Monte Carlo simulations to generate Gunn-like oscillations in the terahertz range [1]. Basically, the slot diode is a high-electron mobility transistor (HEMT) without gate. A schematic of the slot diode is shown in Fig. 1. A recess in the cap layer is used to focus the potential drop from source to drain. This focusing of the electric field enables ballistic acceleration of Γ-valley electrons under the recess, reaching speeds exceeding the saturation velocity. When the acceleration voltage equals the energy separation of the Γ- and L-valleys, electrons leaving the recess are pushed into the L-valley. A region of low concentration of fast Γ-valley electrons accompanied by an increased electric field traverses the recess-drain region. With the potential dropping at the recess edge, the cycle is restarted. See Ref. [1] for details.

In this study, InGaAs-based slot diodes have been designed and fabricated. The DC results have been compared with the static I-V simulations reported in Ref. [1].

2. EXPERIMENTAL

Diodes were fabricated on an epitaxial structure on semi insulating InP bulk similar to a traditional InP HEMT epitaxial structure [2]. An InGaAs/InAlAs channel was used, as shown in Fig. 1. A planar Si-delta doping layer of 5x10^{12} cm-2 in the InAlAs barrier provided the electrons for the InGaAs channel. The channel consisted of 65% indium alloy. On the top was a 20 nm thick highly doped InGaAs cap layer.

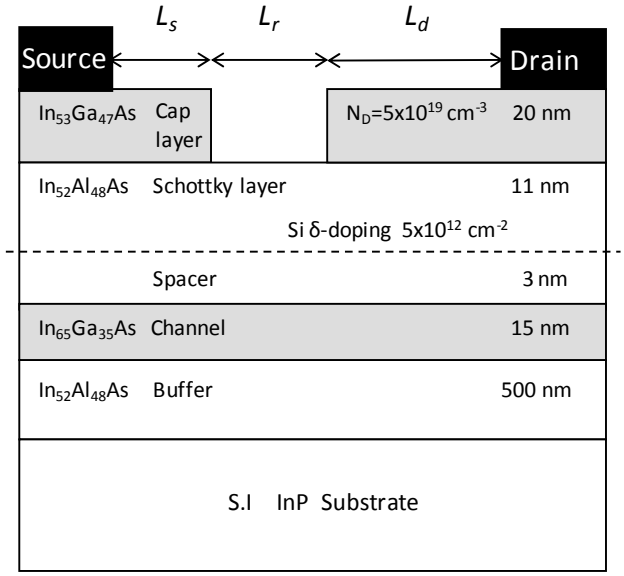

Fig. 1: Schematic view of the slot diode including epitaxial structure.

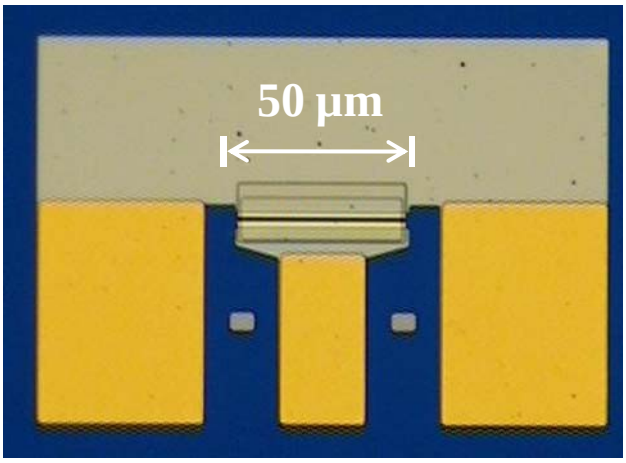

Fig. 2: An optical microscopic view of a slot diode designed in a coplanar layout. The device width is 50 µm.

Hall measurements at 300 K revealed a channel electron mobility of more than 11,600 cm^2/Vs and a sheet carrier concentration of 3.18x10^{12} cm^{-2}. Sheet resistance was 59 and 620 Ω/sq, with and without the cap layer, respectively.

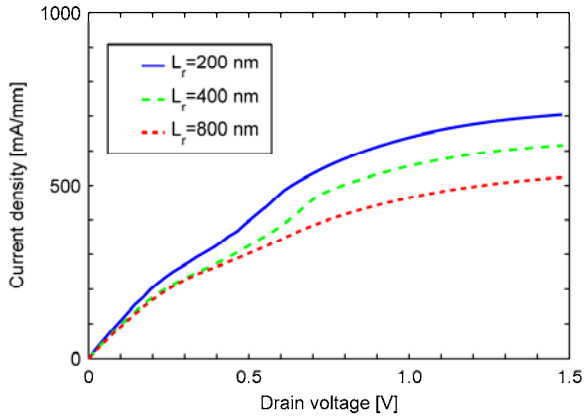

Fig. 3: Current versus drain voltage for different L_r. (L_s=200 nm, L_d=550 nm)

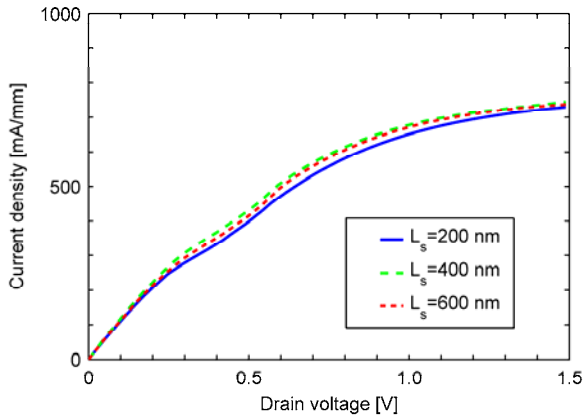

Fig. 4: Current versus drain voltage for different Ls. (L_r=200 nm, L_d=550 nm)

Slot diodes were designed with three layout parameters as shown in Fig. 1: Source-recess distance L_s, recess length L_r and recess-drain distance L_d. Distances L_r and L_d are expected to influence the oscillation frequency of the final slot diode while distance L_d acts as a series resistance [1].

Ohmic contacts were fabricated using a three-metal Ni/Ge/Au (100/520/820 Å) stack. Following rapid thermal anneal, contact resistance was < 0.09 Ωmm. The recess in the cap layer was defined by e-beam lithography using ZEP-resist and etched with a succinic acid/hydrogen peroxide (9:2) solution. Finally, evaporated gold contacts were defined followed by a Si_3N_4 PECVD passivation of the slot diodes. A top view of a fabricated slot diode with a width of 50 um is presented in Fig. 2.

3. RESULTS

On-wafer DC measurements were performed in a dark environment. In Figs. 3, 4 and 5, the output current density of the slot diode is shown as a function of drain voltage up to 1.5 V for the design parameters L_r, L_s and L_d, respectively.

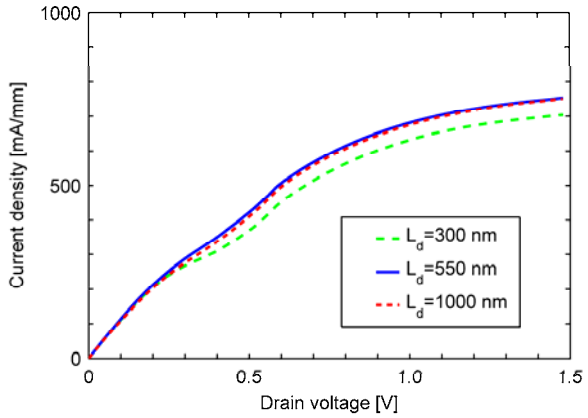

Fig. 5: Current versus drain voltage for different L_d. (L_s=200 nm, L_r=200 nm)

All curves show a tendency for saturation around 750 mA/mm. However, for increased L_r, the saturated current is reduced; see Fig. 3. For L_d and L_s, the output current density is largely unaffected. The recess length has greatest influence, which is understood by the higher resistance of the recess region in relation to the source/drain regions.

All curves exhibit a kink in the I-V curve around 0.5 V drain voltage. A kink has been predicted in Ref. [1] for the simulated static I-V characteristics from slot diodes. The simulated slot diodes had a 70% indium composition in the channel, and a delta-doping concentration of $6x10^{12}$ cm^{-2} and a 10 nm cap layer doped with $6x10^{18}$ cm^{-3}. Compared with the simulated curves, the experimental currents in Fig. 4-6 were around 50% lower. Ultimately, direct detection through RF measurements must be performed to confirm the existence of terahertz oscillations.

4. CONCLUSIONS

Slot diodes based on an InGaAs/InAlAs HEMT structure have been fabricated using three lateral design parameters. The DC output current density showed a slight kink around 0.5 V drain voltage. The recess length was found to be the only design parameter to significantly influence the magnitude of the output current.

ACKNOWLEDGEMENT

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CHARACTERIZATION OF InSb MOS DIODES ON Si SUBSTRATES PREPARED BY SURFACE RECONSTRUCTION CONTROLLED EPITAXY

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ABSTRACT

Al_2O_3/InSb MOS diodes were fabricated to investigate the possibilities of InSb MOSFETs on Si substrates. The InSb layers were grown by MBE using surface reconstruction controlled epitaxy technique. This technique is based on the finding that the InSb layer grown on a Si (111) substrate is rotated by 30 degrees with respect to the substrate under a certain condition. This rotation drastically reduces the lattice mismatch from 19.3 % to 3.3 %. Owing to this novel growth technique, good *C-V* characteristics showing inversion and accumulation were demonstrated.

1. INTRODUCTION

Recently, III-V compound semiconductors have been attracted much attention as a channel material for MOS transistors in the post scaling era. InSb is one of the most promising candidates because it features highest electron mobility of 78,000 $cm^2/(Vs)$ and high saturation velocity of $5x10^7$ cm/s. High performance HEMTs based on InSb/InAlSb material system have been already demonstrated [1]. However, growth of high quality InSb on Si is difficult due to the large lattice mismatch of 19.3%. So far, most of the devices reported were grown on GaAs substrates.

Most recently, we have demonstrated that good InSb epitaxial films can be grown on Si (111) substrates using MBE via InSb bi-layer with special care to the surface re-construction [2]. Extremely high mobility of 38,000 $cm^2/(Vs)$ was obtained for relatively thin (1.2 μm) InSb on Si [3]. In this paper, we report on Al_2O_3/InSb MOS diode characteristics fabricated on InSb films grown on a Si (111) substrate using this technique.

2. SURFACE RECONSTRUCTION CONTROLLED EPITAXY

Our growth technique is based on the finding that the InSb layer grown on a Si (111) substrate is rotated by 30 degrees with respect to the substrate under a certain initial condition [2]. Fig. 1 shows the schematic view of the Si atoms in a (111) surface with two InSb unit cells, non-rotated and rotated ones. As seen in the figure, 30-degree rotation drastically reduces the lattice mismatch from 19.3 % to 3.3 %. This reduction much improves crystal quality of the epitaxial layers.

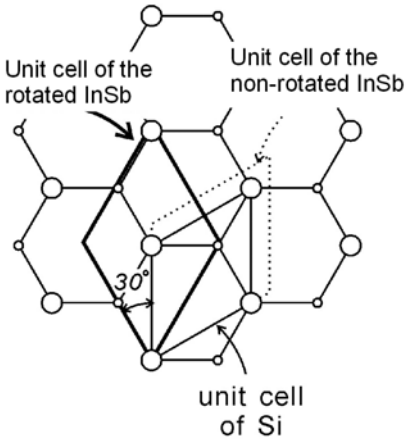

Fig. 1: Schematic view of the Si atoms in a (111) surface with rotated and non-rotated InSb unit cells.

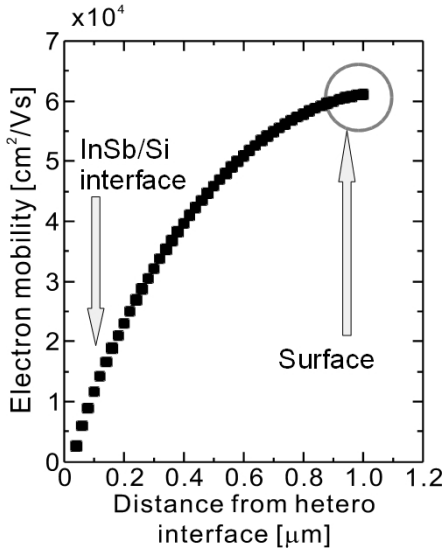

Fig. 2. Depth profile of the electron Hall mobility.

The details of the growth procedure were reported previously [3]. Here, we describe the essence of the growth technique. A key to rotate the InSb epitaxial layer is the InSb initial bi-layer prepared by adsorption of 1 monolayer (ML) Sb onto In-induced surface reconstruction. Special care is taken here to the phase of the surface reconstruction. The InSb films were then grown by two-step growth procedure on this bi-layer.

The growth temperature was 200 C for the first layer, and 440 C for the second layer, respectively.

The grown InSb films (thickness 1-μm) were slightly n-type though no impurity was intentionally doped. The electron concentration and the electron mobility were around $2x10^{16}$ cm^{-3} and 38,000 $cm^2/(Vs)$, respectively. Fig. 2 shows the mobility profile of the grown sample, which was obtained by the differential Hall measurement. Ultra high mobility of 60,000 $cm^2/(Vs)$ was obtained near the surface [4].

3. Al_2O_3/InSb MOS DIODES

We fabricated Al_2O_3/InSb MOS diodes on the epitaxial films grown using above technique [5]. An Al_2O_3 insulator was deposited by using atomic layer deposition (ALD) at 250 C. Thickness of the Al_2O_3 was 30 nm. Two types of ohmic contacts were used for InSb, Ti/Au non-alloyed contacts and Au/Ti/Ni/Au/Sn alloyed contacts. The diodes were circular with diameters of 100 μm.

Fig. 3 shows the capacitance-voltage curves of the fabricated diode with non-alloyed contacts measured at room temperature. When the applied voltage is 2.5 V, the capacitances are close to the accumulation capacitance assuming the Al_2O_3 dielectric constant of 10. The *C-V* curves are symmetric, and show a minimum at about 0V. These curves imply that the inversion occurs at negative bias together with the electron accumulation for positive bias. However, the capacitance drop at the center dip is small, only about 10 %. This is in contrast with the value expected from the Debye length, which is approximately 40%. This is probably due to the high generation-recombination rate for the narrow bandgap InSb as well as the interface states. Very similar *C-V* curves have been reported for Al_2O_3/InAs MOS diodes [6].

Then, we measured *C-V* characteristics at 77 K to investigate the effect of low generation-recombination rate. The results are shown in Fig. 4. The drop at the center dip increases considerably and the *C-V* curves resemble that of conventional Si-MOS diodes. This is consistent with the ratio of thermal energy to bandgap. Anyway, these results clearly demonstrate that the interface Fermi level can be controlled from the valence band to conduction band by the gate voltage.

The *C-V* curves at 100 kHz still show low frequency behavior even at 77 K. We think this is due to the Ti/Au non-alloyed ohmic contact, which can work both for electrons and holes. This is problematic when applied to FETs, because it should degrade the subthreshold behavior. We then fabricated the MOS diodes with alloyed ohmic contact based on Au/Ti/Ni/Au/Sn. The measured *C-V* curves are shown in Fig. 5. The asymmetric behaviour indicates suppression of hole injection.

4. CONCLUSION

Al_2O_3/InSb MOS diodes were fabricated on a Si (111) substrate. Owing to the novel growth technique, good *C-V* characteristics showing inversion and accumulation were demonstrated.

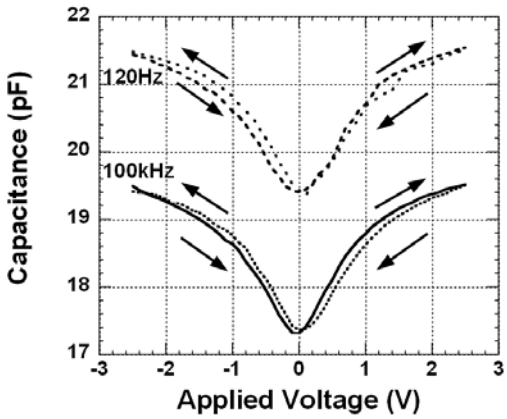

Fig. 3: Capacitance-Voltage curves of the fabricated MOS diodes having non-alloyed contacts measured at RT.

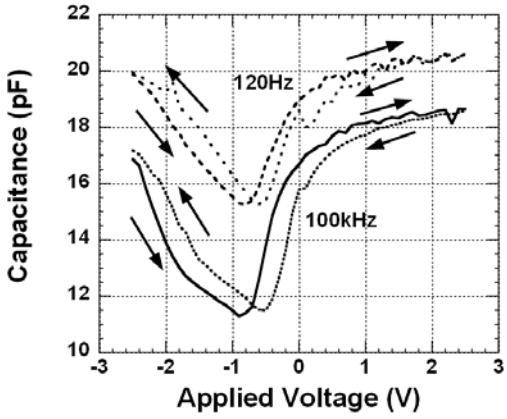

Fig. 4: Capacitance-Voltage curves of the fabricated MOS diodes having non-alloyed contacts measured at 77K.

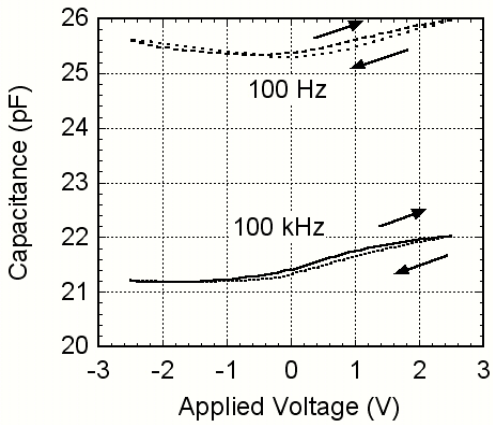

Fig. 5: Capacitance-Voltage curves of the fabricated MOS diodes having alloyed contacts measured at RT.

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DEVELOPMENT OF (In,Ga)As-MOSFETs: HIGH-K GATE STACKS AND OPTIONS FOR INTEGRATION ON SILICON

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For nearly four decades advances in microprocessors have mainly been achieved by scaling down the size and increasing the number of silicon based field effect transistors (FETs). One of the reasons why silicon is so successful is that it possesses a very stable oxide - SiO_2 - which can serve as gate dielectric. However, devices have become so small that intrinsic physical problems like tunneling currents through the gate dielectric have to be tackled. This has already led to the implementation of a non-SiO_2 gate dielectric in the latest microprocessor generations. The International Technology Roadmap for Semiconductors brings up further questions that cannot be answered by scaling anymore. One approach is to change from dimension to material scaling as pioneered by the introduction of the non-SiO2 gate dielectric.

In III-V compound semiconductors, as (In,Ga)As, the electron drift velocity is known to be significantly larger than in silicon. Therefore, III-V materials could be used to increase the performance of FETs without length scaling. Alternatively, the same performance could be achieved at a lower drive voltage, thereby reducing energy consumption and dissipated heat. However, to apply III-V semiconductors for logic some basic challenges have to be faced.

We will present progress in (In,Ga)As surface passivation [1], in gate dielectrics [2] and possible routes towards integration on silicon [3].

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Session 2 :

Microwaves and terahertz devices and technology

Chair : Prof. Dimitris Pavlidis

Monday May 30, 11:00 - 13:00

TERAHERTZ GENERATION IN COMPOUND SEMICONDUCTORS

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ABSTRACT

The generation and detection of terahertz-frequency electromagnetic radiation is of great current interest. Much of this interest lies in the use of ultrafast pump lasers to coherently generate and detect ultrashort pulses of terahertz radiation. There are three main physical mechanisms by which the conversion from pump laser to terahertz radiation occurs, and compound semiconductors turn out to be well suited to each. *Photoconductivity* involves the photoexcitation of electron-hole pairs and their acceleration under an applied external bias; GaAs and related compounds are widely employed for this purpose. *Transient currents* involve the formation of a dipole due to the drift or diffusion of the electrons and holes; a prominent example is InAs. *Optical rectification* is a nonresonant phenomenon depending on the electro-optic coefficients; ZnTe is the best-known example.

1. INTRODUCTION

One terahertz is precisely 10^{12} cycles per second. The term "terahertz" may be used more broadly to signify a span of frequencies around this, for example, the range over the two decades 10^{11} to 10^{13} Hz. Electromagnetic radiation of this frequency falls between microwaves at lower frequency and visible radiation at higher frequency. Terahertz radiation is therefore described as lying between electronics and photonics. Since the methods to generate, manipulate and detect terahertz radiation are less developed than those of electronics and photonics that abut it, the expression "the terahertz gap" has come into vogue. Broadly speaking, terahertz radiation is reflected by metals, transmitted by many common packaging materials such as paper and plastic, and absorbed at characteristic frequencies by polar materials such as water. These characteristics of terahertz radiation open up many possibilities for applications in industrial quality control, non-destructive testing, security, and communications. These applications are driving the development of new terahertz technologies. Terahertz-frequency electromagnetic radiation is sometimes referred to as "MMc", "T-rays" or "T-waves".

Reviews of the field of terahertz technology have been given by Siegel [1] and by Ferguson and Zhang [2]. Monographs have been edited by Mittleman [3], Sakai [4] and Dexheimer [5] and written by Ganichev and Prettl [6], Lee [7] and Zhang and Xu [8]. The field is relatively new and developing [9, 10], and much key information is still found only in the primary research literature.

2. MAKING AND USING ULTRAFAST TERAHERTZ PULSES – TIME-DOMAIN SPECTROSCOPY

While there are many methods of producing terahertz-frequency electromagnetic radiation, the particular method of generating the radiation using a pump laser pulse and using the same pump laser pulse for the detection, has given rise to the method of time-domain spectroscopy which will be the focus of this paper. A schematic time-domain spectroscopy set up is shown in Fig. 1.

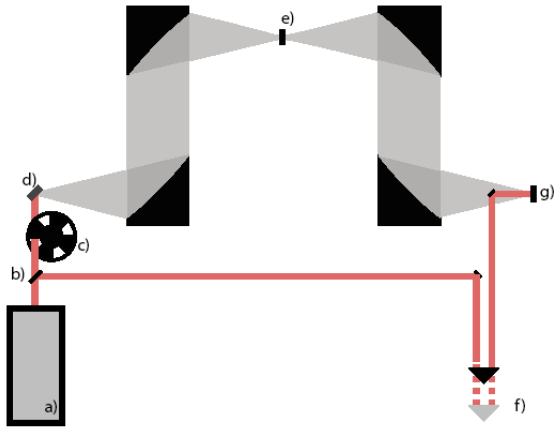

Fig. 1: Terahertz time-domain spectroscopy apparatus. The principal components are (a) pump laser that provides ultrashort pulses; (b) beam splitter to separate pump and probe beams; (c) mechanical chopper; (d) terahertz emitter; (e) sample under study; (f) delay stage which retards the probe beam relative to the pump beam; (g) detector of terahertz radiation [11].

The primary data collected is the terahertz electric field as a function of the movement of the delay stage. This may be regarded as a function of stage travel or, more usually, as a function of delay time. Some typical data sets of time-domain data are shown in Fig. 2.

The time-domain data is then transformed, by Fourier transformation, to yield the frequency-domain data, or usual spectrum. The inset of Fig. 2 gives the spectrum resulting from the Fourier transform of the data.

A great advantage of the time-domain method is that not only the amplitude, but also the phase, of the terahertz field is detected. The real and imaginary components of the optical constants may then be determined directly.

This paper will now concentrate on the development of suitable terahertz emitters, element (d) in Fig. 1.

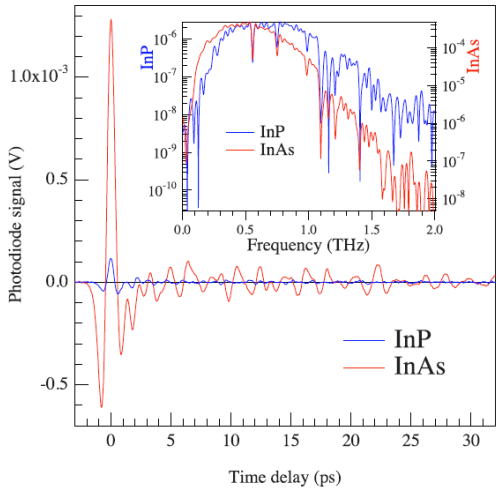

Fig. 2: Terahertz time-domain spectrum obtained from the apparatus shown in Fig. 1. Inset: Terahertz frequency-domain spectrum, obtained from the Fourier transform of the main figure. The signals from two different emitters are shown [12].

3. PHOTOCONDUCTIVITY

A photoconductive emitter relies on the excitation radiation promoting electrons across the bandgap and so producing free carriers, known as photocarriers. The commonly used Ti:sapphire lasers operating at ~800 nm wavelength require an emitter material with bandgap below ~1.5 eV. Lasers operating at communications wavelengths (~1.5 μm) require an emitter with bandgap less than ~0.8 eV. A suitable bandgap is the fundamental requirement of a photoconductive emitter.

The photocarriers are then accelerated in an applied bias field. The more mobile the photocarriers, the greater the effect. Increasing the bias may increase the acceleration up to a point, but if the bias is too great, dielectric breakdown occurs. Thus desirable materials properties for photoconductive emitters are (a) high carrier mobility, (b) high dark resistivity, (c) high breakdown field and (d) short carrier lifetime. In practice, this combination of characteristics means that the most common photoconductive emitter material is low-temperature grown GaAs.

4. TRANSIENT CURRENTS

In a photoconductive emitter, a transient current is made to flow by the application of an external bias. However, there are internal mechanisms by which photocarriers may constitute a current without an external bias. These include currents induced by surface electric fields due to band bending at the material surface and currents induced by differential diffusion of electrons and holes, the photo-Dember effect. Figure 3 shows that the sign of the terahertz signal emitted from InP flips as the doping changes from *n* to *p* type. This is indicative of a transient current controlled by a surface field. In contrast, the photo-Dember effect does not change sign with doping polarity, as it depends only on the relative rate that electrons and holes migrate away from the surface.

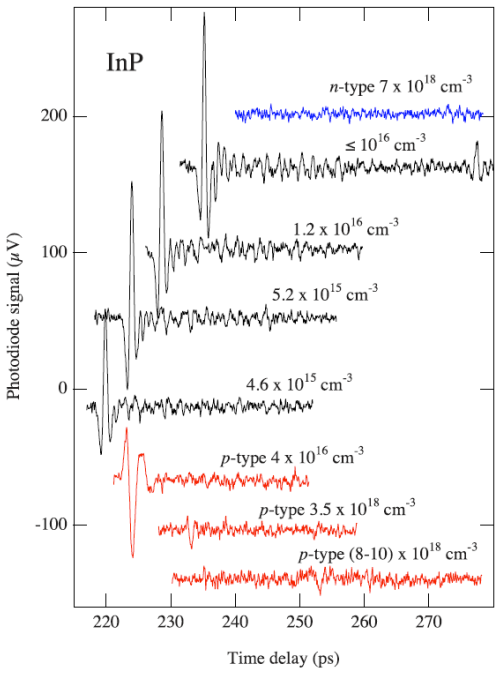

Fig. 3: Dependence of terahertz signal on doping. The time-domain spectra are all from (100) InP samples under identical excitation conditions. Successive spectra have been offset along both axes for ease of comparison, but the scaling is the same for all samples. Note that the terahertz field changes sign as the doping changes from *n* to *p* type. Note also that the most heavily doped emitters, whether *n* or *p* type, are the poorest terahertz emitters [12].

Another indicator of a transient current effect is that it is influenced by an in-plane magnetic field. An example is shown in Fig. 4. The Lorentz force on the photocarriers provided by the applied magnetic field will produce a motion that for some orientation will exactly add to and for the opposite orientation exactly subtract from the terahertz signal produced in the absence of the magnet. A third signature of transient currents, shown in the inset of Fig. 4, is that carrier screening means the terahertz signal tends to saturate as fluence increases.

5. OPTICAL RECTIFICATION

Contrast Fig. 5 for GaBiAs with Fig. 4 for InP. InP shows a strong, systematic variation in terahertz emission with the angle of the in-plane magnetic field; GaBiAs shows none. InP exhibits saturation of the terahertz emission as the excitation fluence increases, GaBiAs does not. These data suggest that transient currents are not playing a role in GaBiAs - although terahertz radiation is being emitted.

Figure 6 provides an important clue as to the origin of the terahertz radiation in GaBiAs. As the azimuthal angle of the excitation radiation is varied, the terahertz emission systematically varies. This indicates a mechanism related to the crystal structure itself, rather than to the photocarriers. Similar effects are observed in porous

material [14]. This mechanism is the nonlinear effect of optical rectification. Detailed analysis shows that the geometry of the excitation radiation relative to the crystal axes (Fig. 7) plays a major role in optical rectification (Fig. 8).

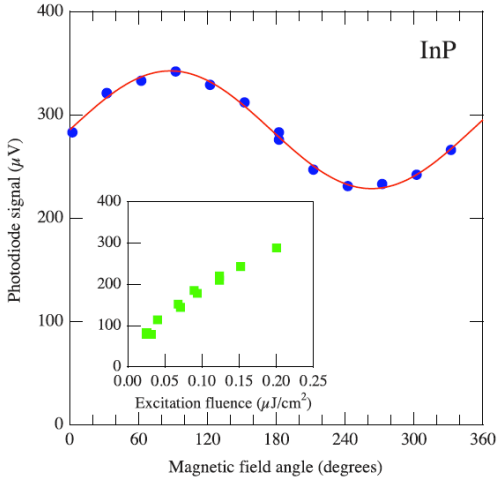

Fig. 4: Effect of varying in-plane magnetic field (main panel) and excitation fluence (inset) on the terahertz emission from nominally undoped InP [12].

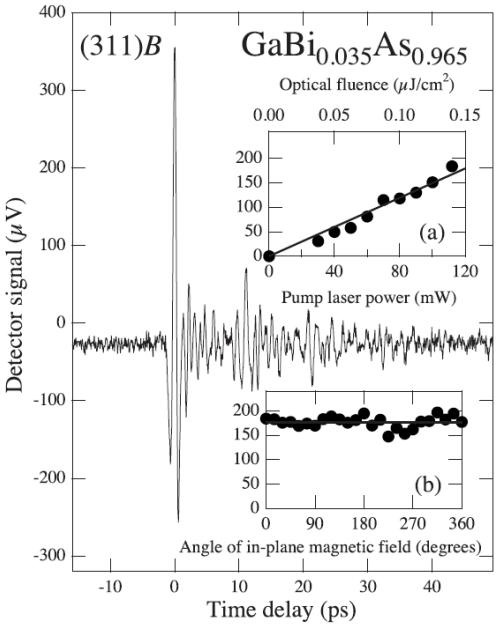

Fig. 5: The time-domain spectrum of terahertz emission from GaBiAs (main panel) and the effect of varying in-plane magnetic field (bottom inset) and excitation fluence (top inset). In contrast to Fig. 4, there is no distinct dependence on angle of the magnetic field and the dependence on pump fluence shows no sign of saturation [13].

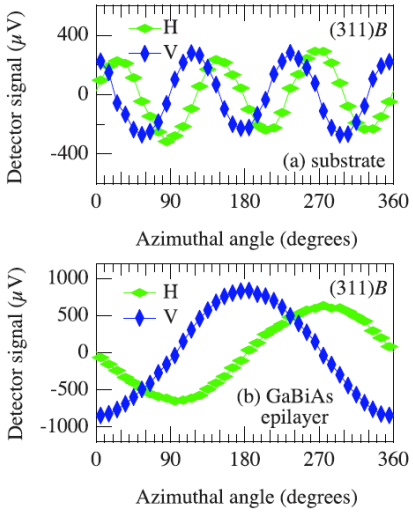

Fig. 6: Variation of terahertz signal as a function of azimuthal angle for (a) GaAs substrate and (b) GaBiAs epilayer grown on the substrate. Apart from the distinctively different azimuthal angle dependence, note the stronger signal from the epilayer. The (green) horizontal diamonds are for the *p* or horizontally polarized signal. The (blue) vertical diamonds are for the *s* or vertically polarized signal [13].

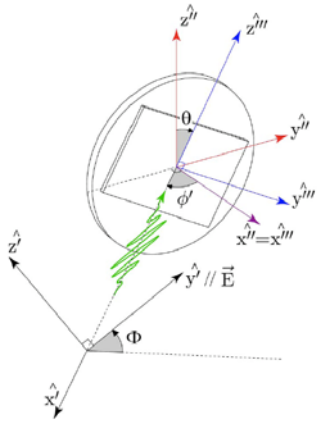

Fig. 7: Geometrical factors that influence the terahertz radiation emitted through the mechanism of optical rectification. These include the angle of incidence, the angle of polarization and azimuthal angle of the excitation radiation relative to the crystal face of the emitter crystal [15].

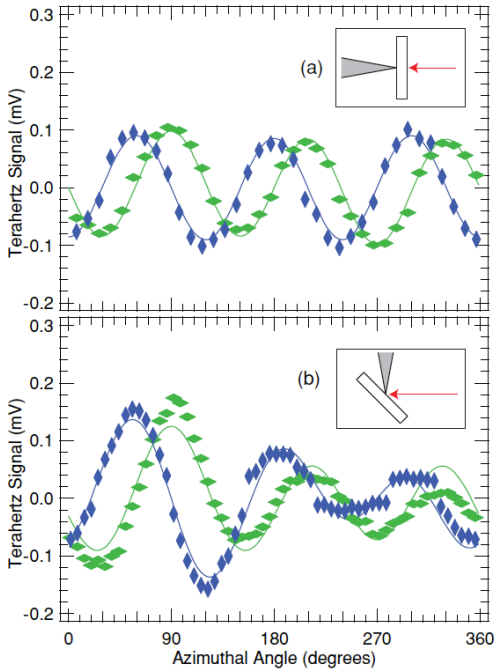

Fig. 8: Two simple emitter geometries, (a) transmission and (b) quasireflection, illustrating the noticeable change this produces in the emitted terahertz radiation as a function of azimuthal angle. The particular data is for (115)A face of GaAs. The (green) horizontal diamonds are for the *p* or horizontally polarized signal. The (blue) vertical diamonds are for the *s* or vertically polarized signal [16].

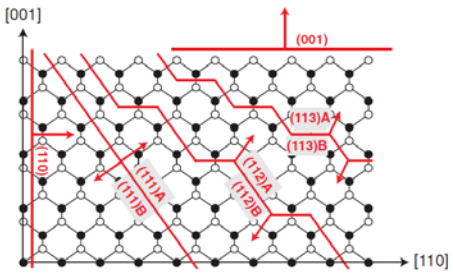

Fig. 9: The III (open circles) – V (filled circles) zincblende structure illustrating the A (open circle rich) and B (closed circle rich) planes. Due to symmetry, there is no need to distinguish A and B faces in the case of (001) and (110) planes [16].

In Fig. 8 it is seen that quite a different azimuthal dependence is exhibited by the same sample in transmission than in reflection geometry.

The geometrical effects are far-reaching. For example, there is a distinction between the A (group III rich) and B (group V rich) faces of III-V semiconductors. (The labeling of the faces is illustrated in Fig. 9.)

In Fig. 10, it is seen that the A side of a (111) GaAs sample acts differently to the B side. This is accounted for by considering that not only the bulk of the sample (common to both) contributes to the optical rectification, but also the surface. In one case these two contributions add, in the other case they subtract.

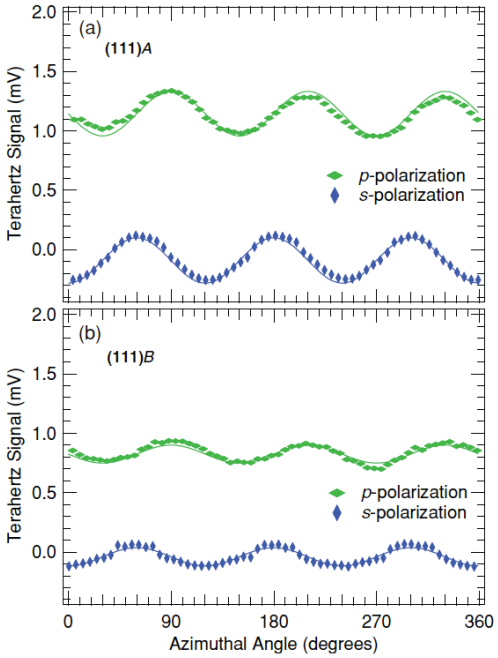

Fig. 10: The terahertz signal from GaAs (111)A and (111)B faces. The (green) horizontal diamonds are for the *p* or horizontally polarized signal. The (blue) vertical diamonds are for the *s* or vertically polarized signal. In each case the *p* signal is offset from the zero by a large transient current component, whereas the *s* signal shows the effect of optical rectification alone. For the A face, the surface optical rectification adds to the bulk optical rectification effect to result in a greater overall signal; for the B face, the surface and bulk terms tend to cancel each other out [16].

6. CONCLUSION

The special properties of compound semiconductors have meant that they dominate the role of emitters of terahertz radiation under excitation by ultrashort pulses of near-infrared radiation. The most common photoconductors are fabricated on LT-GaAs. Many III-V materials act as transient-current emitters; p-InAs is often employed. Studies of high-index GaAs A and B faces have explicated the role that geometrical factors play in optical rectification and allow the surface and bulk contributions to optical rectification to be separated. GaP, CdTe and ZnTe are other commonly used emitters based on optical rectification.

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ELECTRO-OPTIC DETECTION OF CONTINUOUS WAVE THz RADIATION

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ABSTRACT

Photonic techniques for generation and detection of THz radiation are considered to be superior to other techniques with respect to bandwidth and tunability. Especially continuous wave (cw) systems offer high frequency resolution over a large bandwidth which is necessary for spectroscopic applications like detection of narrow gas absorption lines. This paper presents a continuous wave THz detector based on the electro-optic or Pockels effect working at an optical wavelength of 1.53µm. By using the nonlinearity of a <110> GaAs crystal the homodyne detection in a photoconductive THz system is demonstrated.

1. INTRODUCTION

In the past, photoconductive THz-systems were mainly based on an optical wavelength of 800nm, because LTG-GaAs is the common material for photoconductive devices. A new trend pushes the optical wavelength to 1.5µm. This allows making use of mature components developed for optical communications. While high power THz emitters like UTC diodes are available at this wavelength, sensitive detectors are still quite rare.

The electo-optic or Pockels effect describes a phenomenon in which the dielectric properties of a crystal are changed by an externally applied bias electric field. In case of a THz detector, the electric field of the incoming THz beam alters the refractive index of the crystal. By probing the refractive index with the optical beat signal, amplitude and phase of the THz signal can be recovered. This allows phase sensitive detection of coherent radiation. Electro-optic detection is very widespread in pulsed photoconductive THz systems [1,2,3], but relatively unknown in cw systems [4].

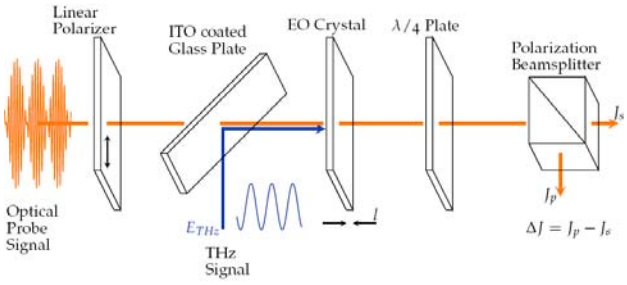

Fig. 1: EO Detection scheme: THz beam and optical probe beam travel collinear through the EO crystal that has a length *l*.

2. ELECTRO-OPTIC DETECTOR

The optical path of the realized detector is implemented in free space as shown in Fig. 1. The optical beat signal travels through a linear polarizer before it is superimposed with the THz beam. Both beams have to be collinear on the EO crystal. This is achieved by an ITO coated glass plate: In the THz range it acts as a mirror while it is transparent in the optical range. A <110> GaAs plate with a thickness of 1.5mm acts as EO crystal. The electric field of the THz beam causes a change of the polarization of the probe beam. This change can be expressed as a change of the intensity between both polarization components [3]:

$$\Delta J = J_0 \frac{\pi n_{opt}^3 E_{THz} r_{41} l}{\lambda_{opt}} \quad (1)$$

where n_{opt} denotes the refractive index at the optical wavelength, E_{THz} the electric field of the THz-wave, l the thickness of the crystal and r_{41} the nonlinear optic coefficient of the crystal. For GaAs this value is 1.5pm/V [1]. Maximum detection is achieved when the angle between the polarization of the THz beam and the polarization of optical beam is 0° or 90°. To prevent standing waves of the optical signal inside the GaAs crystal a SiO_2 antireflection coating has been deposited on both sides the crystal.

The polarization change is detected via a polarization splitter in combination with a difference photodetector. A quarter wave plate between the EO crystal and the polarization splitter is used to equalize both polarization components at the detector. This allows removing the DC part from the difference signal.

The detected signal can be enhanced by using a longer interaction length l. For constructive interference the phase relation between the optical beat signal and the THz wave has to be constant over the whole interaction. Due to the wavelength dependency of the refractive index this condition can be hold only over a limited length. The coherence length is inversely proportional to the THz frequency f_{THz} [1]:

$$l_c = \frac{c_0}{2 f_{THz} \left| n_{THz} - n_{opt} \right|} \quad (2)$$

The refractive properties of GaAs have been investigated in the optical [5] and THz range [6]. Using these values a coherence length of 1.5mm at 460GHz can be calculated for the realized detector. Higher frequencies can be achieved by using a thinner crystal with the drawback of lower responsivity.

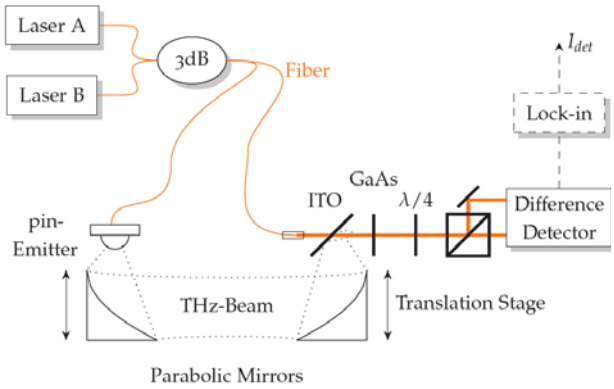

Fig. 2: Schematic of the experimental setup: The electro optic detector consists of an ITO beam combiner, a GaAs crystal and a quarter wave plate in front of a polarization splitter.

3. EXPERIMENTAL SETUP

The experimental setup is shown in Fig. 2. The optical path consists of two continuous wave laser sources and a fiber based 3dB combiner/splitter. By changing the wavelength of the lasers, the beat frequency f_{THz} can be tuned between 0 and 900GHz. The combined optical power at each output of the splitter is 12mW.

The generation of the THz signal is done by a pin-diode based emitter [7]. The emitter has an output power of 3µW at 200GHz, at higher frequencies it drops down due to RC and transit time limitations. The THz-beam is focused on the detector via two off axis parabolic mirrors. By moving the parabolic mirrors the phase relation between THz beam and probe beam at the detector can be changed. The slight misalignment of the focus due to the movement does not affect the measurement. By modulating the amplitude of the emitter signal the Lock-in technique can be applied to lower the noise floor.

4. EXPERIMENTAL RESULTS

Fig. 3 shows the measurement result at f_{THz}=200GHz. Due to a change of the phase relation by moving the mirrors the detected signal shows a sinusoidal behavior:

$$I_{\det} \propto J^0_{opt} E^0_{THz} \cos(2\pi f_{THz} \Delta d / c_0) \quad (3)$$

The amplitude of the modulated signal is 250nA. Compared to the DC part of the detected photocurrent of 380µA this results in a fraction of the modulation of $\Delta J/J_0$=~6.6x10^{-7}. Using Eq. (1) the electric field at the GaAs crystal is calculated to be 3.7V/m.

The frequency of the measured signal corresponds to the wavelength of the beat signal which is 1.5mm. Amplitude and phase of the THz signal can be found via curve fitting.

In a second measurement a glass sample of 1mm thickness has been positioned in the THz beam. This induces a phase change of $\Delta\varphi=0.87\pi$ which corresponds to a refractive index of 1.98.This is in good agreement to values reported in literature [8].

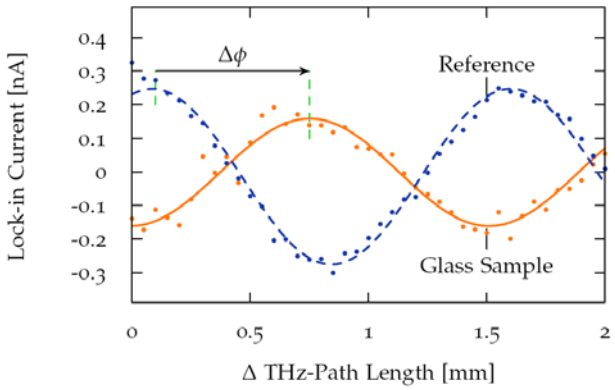

Fig. 3: Detected signal versus delay of the THz signal at 200GHz for empty THz path and with a glass sample.

5. CONCLUSIONS

Electro optic detection of continuous wave THz signals in a photoconductive system has been demonstrated for the first time at 1.53µm optical wavelength. The homodyne detection gives phase information; this allows the estimation of dielectric properties of materials as it has been shown for a glass sample.

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MICROWAVE CIRCUITS AFFECTED BY PASSIVE INTER-MODULATION IN COMMUNICATION SATELLITES

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A generally observed problem with microwave circuitry for communication systems is cross-talk between channels. This is often caused by non-linear effects due to active components. However, it is now known that nonlinearity effects can also be identified as passive processes. This is a particularly severe problem with communication satellites so that the European Space Agency is performing and funding studies in this field.

In an effort to clarify this passive inter-modulation (PIM) problem, we had studied together with the company Tesat-Spacecom in Backnang, Germany, the possibility of this microwave behavior due to pressure contacts and identified a passive inter-modulation signal which was affected by mechanical pressure applied [1],[2]. A simulation study of this experimental behavior obtained shows that the non-linear effect is caused by the structural geometries of mechanical ridges and points as created by metal surface milling, when the waveguide ends are fabricated. The PIM signals are modified by the pressure with which the waveguide parts are forced together. It can be shown that current density changes over nanometric dimensions are causing this effect. This is associated with the scattering of electrons in such metal structures. Local thermal effects can also play a role. Often the phenomena of tunneling Metal- Insulator-Metal transitions (as created for example by the formation of native oxides during the fabrication in the workshop), exhibit the non-linearity. Of course this always occurs within the skin-effect of the microwave current density versus its electric field.

Microwave transmission is generally described by equivalent components of L, C, R and G with the usual definitions of these symbols. Each of them can show correspondingly a non-linearity of current versus voltage. The identification of many further possible non-linear cases is part of our study.

Indeed, interpretations are provided now to explain many cases where PIM has been reported. The surface compositions of native oxides and other materials on metal structures are effective within the skin-effect of microwaves. Also quantum clusters are easily capable of producing PIM effects. Even sharp edges as common with waveguide filters and other components can be responsible for this process. Of course planar wave guides on ceramic substrates are known to generate passive non-linearity effects [3]. All these processes can be expected also with packaged individual components or with integrated microwave circuit structures.

The influence of a large number of PIM effects at metal and insulating surfaces range from wave guiding via active circuitry to antennas in satellites under the very high vacuum conditions present in outer space. It represents a very complex issue which is, however, of particular importance with the increase of communication systems in outer space. There are therefore indications that not only cross-talk problems are caused in this way, but also Bit Error Rates increase of digital systems.

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SiN/AlN/GaN: A PROMISING HETEROSTRUCTURE FOR MILLIMETER WAVE APPLICATIONS

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ABSTRACT

We report on a novel heterostructure based on AlN/GaN capped with an in-situ grown SiN that enables to deliver very high polarization, low leakage current while using ultrathin barrier layers (below 10 nm) without gate insulators. Deep sub-micrometer gate length AlN/GaN HEMTs using this configuration showed the highest output current density above 2 A/mm with high frequency performances and a record extrinsic transconductance close to 0.5 S/mm of any GaN-based devices grown on Si substrate.

1. INTRODUCTION

The dimensions of GaN-based devices need to be reduced in order to increase their frequency range and benefit from their outstanding properties for millimeter wave applications. In particular, the gate length scaling must be linked to the reduction of the gate to channel distance in order to avoid short channel effects [1]. Additionally, high current density should be maintained while downscaling the device geometry. Unlike GaAs or InP-based devices, recessed gate is not a straightforward implementation. Since wet etching cannot be applied (no chemical etchant is known to have a significant etch rate on III-Nitride), dry etching techniques need to be used to remove part of the barrier layer. The etch rate for the typically used Cl_2-based plasma is difficult to control and reproduce. Moreover, dry etching of group-III nitrides is known to cause an increase in the density of surface states which in turn cause dispersion effects. Also, dry etching introduces a lot of defect states, resulting in a Schottky gate with high leakage current. Another approach to achieve high aspect ratio consists in decreasing the barrier thickness. However, decreasing the AlGaN barrier thickness below 10 nm leads to a strong degradation of the two dimensional electron gas (2DEG) carrier concentration [2], resulting in poor device performance. In this frame, we propose a novel ultrathin barrier heterostructure based on SiN/AlN/GaN that allows achieving high aspect ratio with deep sub-micrometer gate length, high polarization and low leakage current.

2. RESULTS AND DISCUSSIONS

The in-situ MOCVD grown SiN cap layer plays a major role in the successful development of this configuration by preventing strain relaxation and enhancing surface quality and robustness [3].

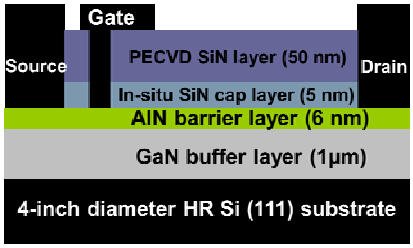

Fig. 1: Cross section of the fabricated AlN/GaN-on-Si HEMTs

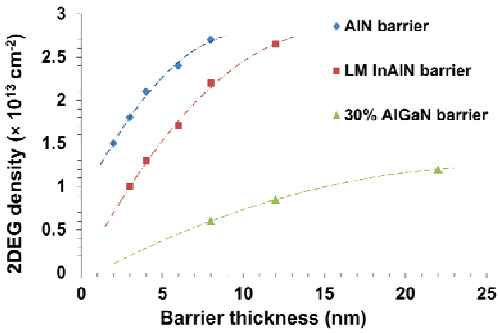

Fig. 2: 2DEG carrier density of various heterostructures as a function of the barrier layer thickness.

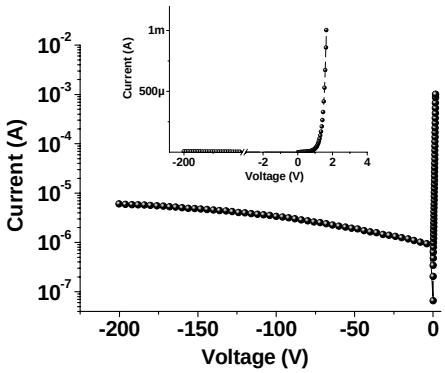

Fig. 3: 50 µm circular diode characteristic of ultrathin barrier thickness AlN/GaN-on-Si heterostructure

A full fabrication process using gate length L_g = 200 nm has been developed on top of high resistive Silicon (111) substrate (see Fig. 1). A Ti/Al/Ni/Au metal stack has been deposited on top of the AlN barrier layer by etching the in-situ Si_3N_4 layer, followed by an annealing at 900°C in N_2 ambient. Device isolation was obtained by He implantation. Gate length of 0.2 µm was defined by conventional e-beam lithography. The SiN underneath

the gate was fully removed using an SF6 plasma etching. Ni/Au gate metals were then deposited. The gate-source and gate-drain spacing were 0.4 µm and 1.3 µm respectively and the device width was 50 µm. Finally, 200 nm PECVD Si_3N_4 has been deposited as passivation layer.

Hall measurements on various barrier thicknesses clearly demonstrate the superiority of the 2DEG properties as compared to the standard AlGaN/GaN and the emerging Lattice matched InAlN/GaN heterostructures, especially for ultrathin barrier thicknesses (Fig. 2). Remarkably low leakage current is observed reproducibly on circular diodes up to 200 V reverse bias indicating that no electron tunneling occurred through the 3 nm ultrathin barrier layer. This is attributed to the absence of defects into the AlN film resulting from the high growth quality as well as the AlN surface quality enhanced by the in-situ grown SiN that prevents oxide and/or defects formation inducing generally parasitic conductions. First device results already show the exceptional potential of this structure. Indeed, an open channel current above 2 A/mm using 6 nm AlN barrier thickness has been achieved (Fig. 4). Excellent small signal parameters (shown in Fig. 5) have been extracted for a 0.2 µm gate length, despite the relatively high access resistances (0.67 Ω.mm) and residual losses most probably located at the buffer/Si substrate interface due to the high lattice mismatched between the two materials. Current gain extrinsic cut-off frequency and maximum oscillation frequency f_T = 52 GHz and f_{max} = 102 GHz at the optimum bias conditions (V_{GS} = -3.2 V and V_{DS} = 5 V), respectively.

Furthermore, record extrinsic transconductance close to 500 mS/mm with 3 nm AlN thickness has been reached (Fig. 6). To the best of our knowledge, these data represent the highest DC characteristics of any GaN-on-Si HEMT. Unlike many reported results corresponding to GaN HEMT with ultrathin barrier layers, it has to be pointed out that device leakage current as low as 10 µA/mm are obtained together with the outstanding mentioned data resulting in device breakdown voltages as high as standard AlGaN/GaN HEMTs.

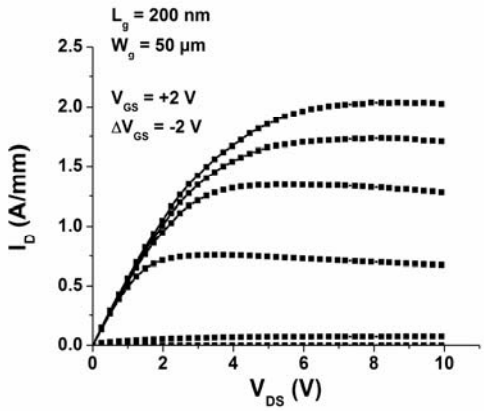

Fig. 4: DC output I_D-V_{DS} characteristics of 2×25 µm AlN/GaN-on-Si HEMT with L_g = 0.2 µm. V_{GS} swept from +2 down to -8 V in 2 V step.

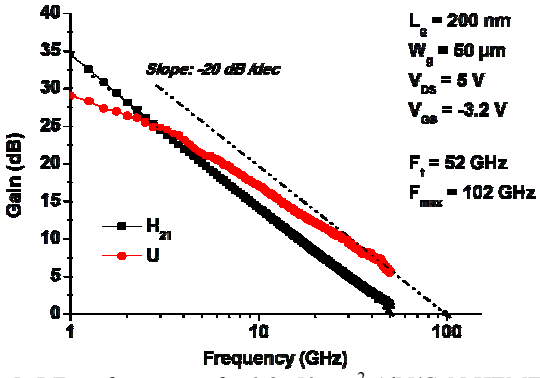

Fig. 5: RF performance of a 0.2×50 µm^2 AlN/GaN HEMT on HR Silicon substrate.

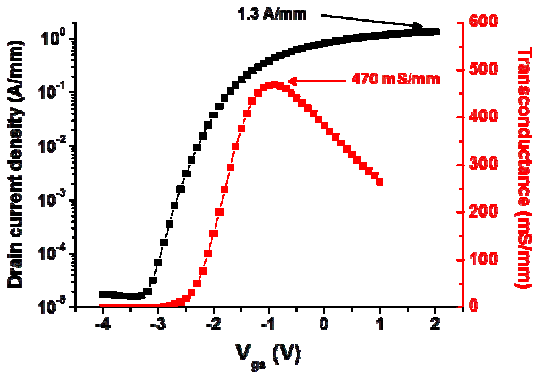

Fig. 6: Transfer characteristics of the 0.2×50 µm2 3 nm barrier AlN/GaN HEMT on Silicon substrate, demonstrating a record extrinsic transconductance of GaN-on-Si HEMTs.

3. CONCLUSION

We have successfully developed a novel SiN/AlN/GaN HEMTs grown by MOCVD on large diameter HR Si (111) substrate. The unique combination of ultrathin barrier layer and high 2DEG density resulted in the highest output current density above 2 A/mm at V_{GS} = +2 V and a record transconductance ever achieved for GaN-on-Si HEMTs together with high frequency performance for L_g = 0.2 µm (f_T = 52 GHz and f_{max} = 102 GHz). Low leakage current is observed in these devices without the use of any gate dielectric, indicating that this planar technology may display high reliability.

The achieved preliminary data make this unique heterostructure an excellent candidate for millimeter wave applications requiring linearity, high temperature, high power or also robust low noise amplifiers in a cost-effective way.

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$Al_{0.5}Ga_{0.5}N$/AlN/GaN HEMTs FOR MICROWAVE APPLICATIONS

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ABSTRACT

The design, growth, fabrication, and performance of scaled (7 nm-barrier) AlGaN/GaN HEMTs are reported. An optimized surface passivation and an Ohmic recess etch yield HEMTs exhibiting 0.72 S/mm extrinsic DC transconductance at a current density of 0.47 A/mm. Devices with a gate length of 90 nm achieve 78 GHz unity-current-gain frequency (f_T) and up to 166 GHz maximum frequency of oscillation (f_{max}). The minimum noise figure, F_{min}, at 10 GHz is 0.52 dB (G_A = 9.5 dB).

1. INTRODUCTION

Thin-barrier HEMTs based on the III–nitride material system are an active area of research for millimeter-wave applications [1]. State of the art approaches involve relatively thick (> 20 nm), $x \sim 25\%$ $Al_xGa_{1-x}N$ barriers [2]; ultrathin (< 4 nm), binary AlN barriers [3]; ultrathin $x = 72\%$ $Al_xGa_{1-x}N$ barriers [4]; and lattice-matched $Al_xIn_{1-x}N$ barriers [5]. Within very high (70–100%) Al composition $Al_x(Ga,In)_{1-x}N$ barriers, a sharp electric field results from polarization-induced charge; this often necessitates an insulated-gate, or MISHFET, approach to ameliorate high gate leakage currents. In this work, an uninsulated $Al_{0.5}Ga_{0.5}N$/AlN/GaN HEMT structure is investigated. The challenges presented by this thin-barrier material are (1) to effectively passivate the surface to mitigate surface depletion and transient trapping effects and (2) to achieve low-resistivity Ohmic contact.

2. MATERIAL DESIGN

To efficiently modulate the 2DEG and minimize short-channel effects, the ratio of the gate length, L_G, to the distance, d, between the gate metal and the center of the 2DEG should be ~15 [6]; in this work, d was scaled to 7 nm. The epitaxial layers were grown by MOCVD on semi-insulating SiC. From the top down, the material consisted of a 20 Å GaN cap, 36 Å $Al_{0.5}Ga_{0.5}N$ barrier, 15 Å AlN interbarrier, a 1.8 µm compensation-doped Fe:GaN buffer, and a s.i. SiC substrate. Schrödinger–Poisson simulations predicted a 2DEG sheet density, n_{s0}, of 1.4×10^{13} cm^{-2}; the AlN interbarrier induces two-thirds of the 2DEG and improves hot-electron confinement, while the $Al_{0.5}Ga_{0.5}N$ barrier layer induces the remaining one-third of the sheet density. The tunneling probability compared to an AlN-only barrier is reduced by the inclusion of the $Al_{0.5}Ga_{0.5}N$ and GaN cap.

Lehighton measurements across the unpassivated 3" wafer revealed a sheet resistance of 405 ± 17 Ω/□. Passivated van der Pauw test structures indicate a sheet resistance R_{sh} = 334 Ω/□, Hall mobility 1245 cm^2/V s, and $n_{s0} = 1.5 \times 10^{13}$ cm^{-2}, demonstrating excellent agreement with the simulations. The realized reduction in sheet resistance indicates effective surface passivation.

3. FABRICATION

After a standard wafer cleaning, the surface of the GaN cap layer was passivated with a ~70 nm LPCVD SiN_x film, which was grown using ammonia and dichlorosilane precursor gases at 820°C and 250 mTorr. The deposition temperature, pressure, and flow ratio were optimized to minimize the interface trap density. Under these growth conditions, the refractive index was measured as 2.3 at a wavelength of 632 nm, indicating a silicon-rich film. The passivation was etched in subsequent mesa isolation and contact deposition steps using an NF_3 ICP RIE. Ohmic contacts were recessed into the $Al_{0.5}Ga_{0.5}N$ barrier layer using a low-bias Cl_2/Ar ICP RIE. The recess depth was characterized as a function of etch time and optimized for minimal Ohmic contact resistance, R_c, achieving $R_c < 0.5$ Ω mm across more than one wafer. A recessed, Ti/Al/Ni/Au metallization yields R_c = 0.48 Ω mm and R_{sh} = 332 Ω/□. These values are tenable for mm-wave applications and an order of magnitude better than our non-recessed contacts (R_c = 4.4 Ω mm, R_{sh} = 340 Ω/□).

Two-finger, U-shaped devices were fabricated. A two-step electron-beam lithography was used to define and lift-off Ni-based, gamma-shaped, field-plated gates.

4. DEVICE CHARACTERIZATION

Characterization included DC, S-parameter, pulsed (DiVA D225 using 200 ns pulses and a 1 ms period), noise parameters (ATN NP5), and RF large signal (Maury LSNA). A dynamic load line is constructed from the waveforms measured directly at six harmonics.

The DC output characteristic of a representative 2×100 µm HEMT with a 170 nm gate footprint, 1 µm

source-gate spacing, 2 µm gate-drain spacing, and a gate pitch of 50 µm (Fig. 1a) shows an on resistance of 2.1 Ω mm and reasonably low output conductance.

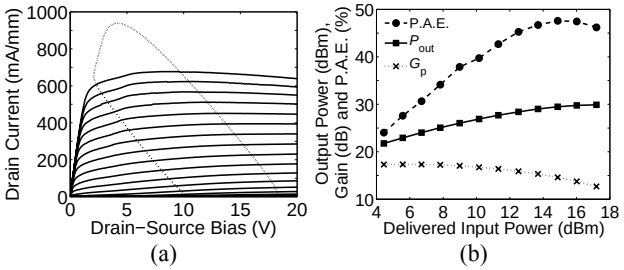

Fig. 1: For a 2×100×0.17 µm HEMT: (a) Output characteristic (solid); the gate voltage is depicted in steps of 0.1 V to V_{GS} = 0.7 V. The load line (dotted) is measured in saturation at 8 GHz CW biased class AB at V_{DS} = 10 V. (b) RF performance at 8 GHz CW, class AB, V_{DS} = 25 V.

The transfer characteristic exhibits good pinch-off at a threshold voltage, V_{po}, of −0.6 V and a peak extrinsic transconductance of 662 mS/mm. The gate bias is limited to V_{GS} < +0.8 V, beyond which the Schottky diode turns on. The breakdown voltage was characterized as V_{DGbr} = 99±8 V and V_{DSbr} = 88±8 V with a criterion of 1 mA/mm. The gate current, $|I_G|$, at V_{po} under cold-FET conditions is < 0.5 µA/mm.

This 2×100 µm device demonstrates a peak unity-current-gain frequency, f_T, of 50 GHz and simultaneous maximum frequency of oscillation, f_{max}, of 55 GHz at V_{DS} = 5.5 V. The latter increases to f_{max} = 105 GHz at V_{DS} = 25 V, while f_T drops to 40 GHz due primarily to thermal effects.

Noise parameter characterization of the same 2×100 µm HEMT with 170 nm gate footprint reveals a minimum noise figure F_{min} < 1 dB through the 14 GHz measurement range (Fig. 2). At 5 GHz, F_{min} = 0.36 dB with an associated gain G_A = 13.6 dB; at 10 GHz, F_{min} = 0.52 dB with G_A = 9.5 dB. These noise parameter results are among the lowest noise figures reported for short-gate III–nitride HEMTs [7].

Pulsed I_D–V_{DS} characteristics reveal negligible gate lag and ~6% drain lag in the knee region. This predicts low DC-RF dispersion under large-signal operation, which is confirmed by the full swing of the dynamic load line [8].

The 170 nm-gate-footprint HEMTs were characterized under power-matched, continuous-wave (CW) class AB operation at 8 GHz. As shown in Fig. 1b, the device delivers 4.9 W/mm with 46% power-added efficiency (P.A.E.) at V_{DS} = 25 V when driven into compression.

The f_{max}/f_T ratio benefits from the reduced access resistance of a shorter source-gate spacing. A 2×50 µm HEMT with the gate footprint scaled to 90 nm and source-gate spacing halved to 0.5 µm exhibits a peak extrinsic DC transconductance of 722 mS/mm at a current density of 0.47 A/mm. At the same bias, f_T = 78.5 GHz and f_{max} = 93 GHz; after de-embedding the pad capacitances, $f_{T,int}$ = 91 GHz. The maximum frequency of oscillation increases to f_{max} = 166 GHz with simultaneous f_T = 57 GHz at V_{DS} = 20 V.

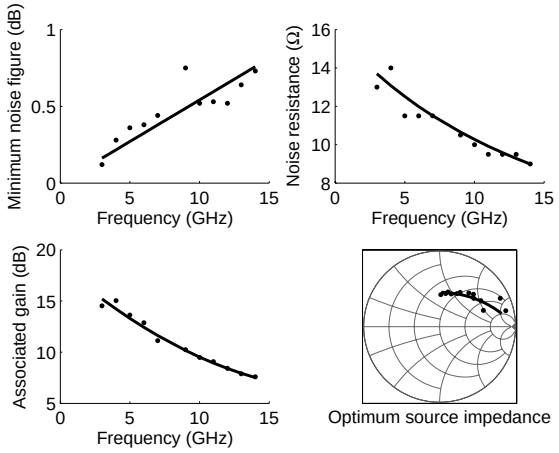

Fig. 2: Noise parameters of a 2×100×0.17 µm HEMT at V_{GS} = −0.1 V, V_{DS} = 5 V (I_D = 177 mA/mm, I_G = −4 µA/mm); curves guide the eye.

5. CONCLUSION

High-Al content AlGaN/GaN HEMT structures with high sheet density and mobility are fabricated using a method compatible with Chalmers' in-house GaN MMIC process. An LPCVD passivation mitigates the surface depletion effect induced by the thin barrier and results in low DC–RF dispersion. A recessed Ohmic contact achieves low contact resistivity. The HEMTs exhibit excellent noise performance and transconductance; the high g_m/I_D ratio allows high gain even at low current densities. The DC, pulsed, small-signal, noise parameter, and large-signal results indicate that this thin-barrier $Al_{0.5}Ga_{0.5}N$/AlN/GaN epitaxial platform is promising for realizing high-power, high-efficiency microwave and mm-wave MMICs, including LNAs, switches, and PAs.

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DESIGN AND CHARACTERIZATION OF GaN HEMT VARACTORS FOR RECONFIGURABLE MMICS

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ABSTRACT

This paper presents varactors based on gallium nitride *(GaN)* HEMT technology. They have been evaluated regarding their absolute capacitance value, tunable capacitance ratio and quality factor. To optimize the varactor performance, several device parameters have been varied and analyzed. An alternative varactor configuration is presented to overcome typical limitations in the device performance due to the chosen semiconductor material.

1. INTRODUCTION

Simultaneous use of different frequency bands in future wireless communication systems increases the need of reconfigurability in microwave backhaul systems. Since cost and space requirements for implementing filters in every frequency band are very high, we study the potential of varactors based on GaN HEMT technology for the use in reconfigurable circuits such as tunable filters, matching networks and phase shifters. For this purpose varactors have been designed using the Chalmers in-house MMIC process. The layout of the varactors has been varied in key parameters to improve the device performance.

2. VARACTOR TOPOLOGY

The varactors are fabricated on an AlGaN/GaN epiwafer with a SiC substrate. The AlGaN thickness is 240 Å. The varactor device topology differs from an original GaN HEMT in the way that source and drain have been intrinsically connected to form the cathode of the varactor. This will simultaneously reduce the occupied area and parasitics. The gate acts as anode.
Several varactor layouts have been fabricated and analyzed to find an optimal trade-off between losses and capacitance tuning ratio. They vary in key parameters as anode length, anode width, anode-cathode distance, field plate and number of anode fingers.
Fig. 1 shows a picture of a fabricated varactor having a gate length of 0.25 µm and gate width of 4x100 µm.

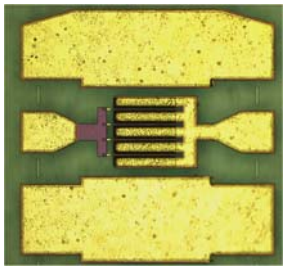

Fig.1: Picture of varactor based on GaN HEMT technology.

3. MODELING

An equivalent circuit has been developed for the GaN HEMT based varactor [1]. It is shown in Fig. 2. Cj and Rj are the voltage dependent intrinsic tunable capacitance and resistance. Cp represents the parasitic pad capacitances and Ls the series, ideally frequency independent, inductance. Cgd and R were added to complete the model, but their effect is practically negligible for these varactors. The in-house fabricated varactors have been modeled using this simplified equivalent circuit.

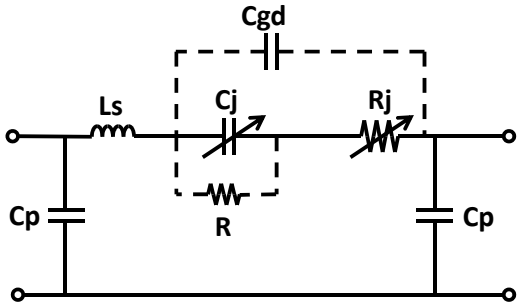

Fig. 2: Equivalent circuit of GaN HEMT varactor.

4. RESULTS

S-parameter measurements have been performed to analyze the fabricated varactors in terms of absolute capacitance value, capacitance tuning ratio and quality factor.
Fig. 3 shows the tunable intrinsic capacitance for four different gate lengths. It can be seen, that the gradient of the C-V curve is very steep. This is a typical limitation of the chosen semiconductor material and will affect the performance of the device. It results in a low voltage

swing. Therefore this varactor configuration could be used as a two-state varactor.
The capacitance value below pinch-off, here called off-state, is similar for the different gate lengths. The absolute capacitance value for the on-state is scaling with the gate length; the longer the gate length, the higher the absolute capacitance value. The maximum available capacitance ratio with this configuration is 5.8, the minimum 1.9. For varactor applications the value below pinch-off is more important.

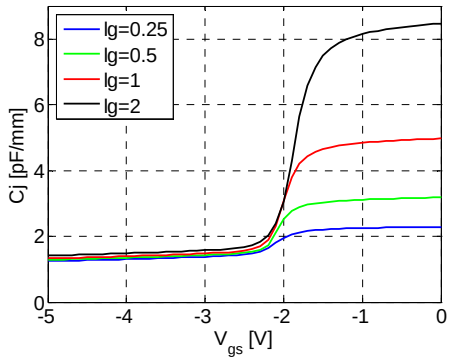

Fig. 3: Intrinsic capacitance for different gate length, gate width = 400 µm.

Fig. 4 shows the quality factor versus frequency for the two-state varactor below pinch-off at Vgs = -6V and above knee voltage at Vgs = 0V. Maximum Q-factor is 32 for low frequencies in off-state. Above 8 GHz, the quality factor is quite low. This could limit the use of GaN HEMT based varactors in future RF applications.

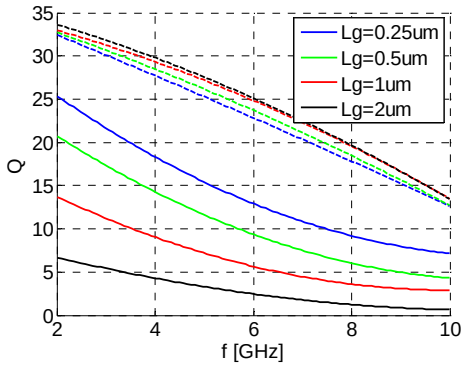

Fig. 4: Quality factor for on-state (solid lines) and off-state capacitance (dashed lines).

5. ALTERNATIVE LAYOUT

An alternative configuration has been considered, shown in Fig. 5, to overcome the voltage swing limitation of the presented varactor. The improved layout contains a standard GaN HEMT with gate length and width similar to the one of Fig. 1. The device is gate-biased below pinch-off, so that the equivalent capacitance seen at the drain side can be modulated by varying the drain-source voltage.

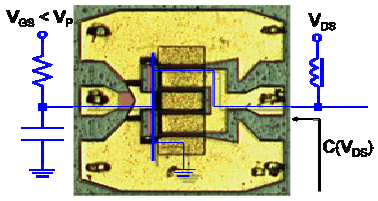

Fig. 5: Picture of new varactor configuration.

The capacitance below pinch-off versus drain voltage behavior can be seen in Fig. 6, together with the corresponding Q-factor at 7 GHz.

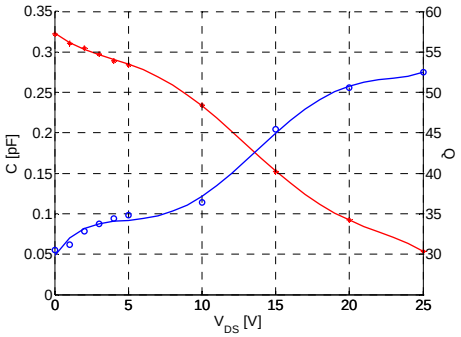

Fig. 6: Capacitance (red line) and quality factor (blue line) extracted from measurements on varactor from Fig. 5.

It can be observed that the Q-factor is generally higher compared to the previous proposed solution. Moreover, aiming for the design of matching networks for power amplifiers, this varactor has the advantage of being able to manage a higher voltage swing. From the C-V curve of Fig. 6 can be observed that a higher applied voltage swing leads to a reduction in the capacitance ratio. This compromise must be evaluated at circuit design level: some techniques, as anti-series varactors, can be adopted to overcome the problem [2].

6. CONCLUSION

Two varactor configurations based on GaN HEMT technology have been presented. Depending on the layout, the quality factor and the capacitance tuning range are influenced.
On the basis of the presented varactor study, reconfigurable circuits will be developed and implemented in the Chalmers in-house MMIC process.

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POWER III-NITRIDE DEVICES WITH FREQUENCY-CONFIGURABLE ELEMENTS

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ABSTRACT

This work reports on a new approach to designing high-speed high-power electronic devices with frequency configurable elements. Such elements behave as conductors at low frequencies and as insulators at high frequencies, thus allowing for independent optimization of DC and RF (or pulsed) performance. We demonstrate the novel approach using microwave switches with "slow gate" leading to low capacitance, HFETs with "slow filed plate" having higher breakdown voltages and other power high-frequency devices.

1. INTRODUCTION

The dilemma of simultaneously meeting the DC/pulse requirements on one side and microwave – on the other is one of the most challenging and well known in semiconductor device and IC design and technology. In recent years, the problem became even more severe as novel devices ought to operate at the conditions close to those imposed by fundamental material limitations. We propose and demonstrate some examples of a new approach to designing high-speed high-power electronic devices with frequency configurable elements. Such elements behave as conductors at low frequencies and as insulators at high frequencies, thus allowing for independent optimization of DC and RF (or pulsed) performance. The proposed novel approach is targeted to not only resolve the above issue but to also bring more functionality to novel microwave, millimeter wave and terahertz devices as well as devices for power electronics, optoelectronics and other emerging fields of modern electronic technology.

2. III-NITRIDE HFETS WITH COMPOSITE FAST/SLOW GATE DESIGN.

In this new device design, there is an additional electrode acting as a "slow gate" formed using low-conducting layer (LCL), which allows for complete removal of the HFET internal capacitance in the OFF state as illustrated in Fig. 1 [1].
When used as a microwave switch, the characteristic charge-recharge time constant of the "slow gate" electrode is configured to be shorter than the switch modulation time but much larger than the period of the operating frequency.

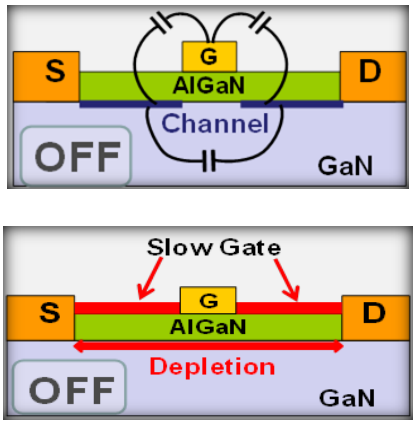

Fig. 1: Conventional (a) and fast/slow gate (b) HFETs in the OFF state [1].

Therefore, the "slow gate" potential is not modulated by the microwave signal and does not add any additional capacitances to HFET microwave parameters. Initial results of using frequency-configurable gate electrode in III-Nitride SPDT RF switch MMIC show significant performance improvement over conventional switch thus confirming the validity of the proposed concept (Fig. 2).

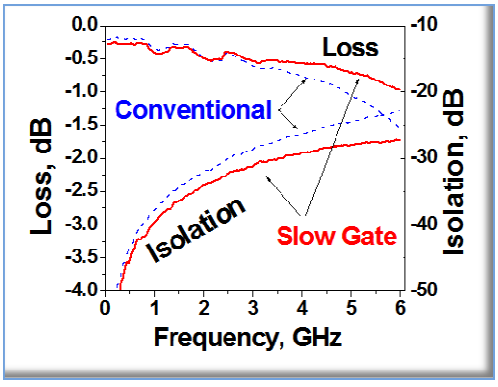

Fig. 2: Characteristics of III-Nitride SPDT switches made using conventional and fast/slow- gate HFETs. The slow gate layer is formed by low-temperature deposited InGaN film [1].

3. FREQUENCY-CONFIGURABLE ELECTRODES FOR ACHIEVING HIGHER POWER.

In power devices, the achievable lowest ON-resistance is in direct contradiction with the obtainable operating voltage. The breakdown problem in these devices is aggravated by strongly non-uniform electric field distribution near the gate edge. Today, the field-plating technique is the only dominating technique that partially smoothens electric field nonuniformity, however field-plated devices suffer from additional capacitances induced by field plates; in addition, the field plate – drain breakdown brings additional limitation into the device performance. A frequency-configurable field-plate (FC-FP) located in the gate-drain spacing of the power HFET or other transistor type allows to achieving almost perfectly uniform field profile yet remaining "invisible" for high-frequency signal and hence not increasing the device capacitance [2].

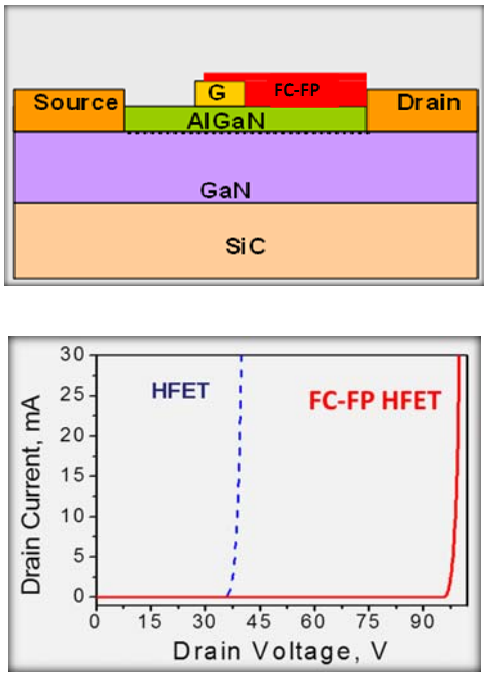

Fig. 3: Initial results on breakdown voltage comparison in conventional and FC-FP HFETs with 1.8 μm gate-drain spacing. The FC-FP is formed by low-temperature deposited InGaN film [2].

Due to nearly unioform electric field profile in the gate-drain spacing, the proposed new design will allow to achieving $R_{ON} - V_{BD}$ relationships in power switches close to the theoretical limit. In RF power amplifiers it allows to break the frequency barrier imposed by the inter-electrode capacitances.

4. FREQUENCY-RECONFIGURABLE ELECTRODES FOR MILLIMETER WAVE – TERAHERTZ ELECTRONICS AND OTHER APPLICATIONS

One of the biggest issues impeding the development of ultra high-frequency electronic devices is severe performance degradation due to inevitable parasitic parameters of transistor access regions. In deep submicron devices and even more importantly in nano-scale gate devices utilizing ballistic effects or plasma waves, source and drain access regions constitute major portion of the total source – drain impedance. The proposed approach of using frequency-reconfigurable electrodes (FRE) with bias-controlled electrode RC-parameters allows for optimal biasing and "pumping" of the devices channel in the access regions, so that required carrier concentration or electric field profile can be obtained (Fig. 4). This will allow for a breakthrough in the achievable cut-off frequencies (especially F_{MAX}) and generated millimeter-wave or Terahertz powers.

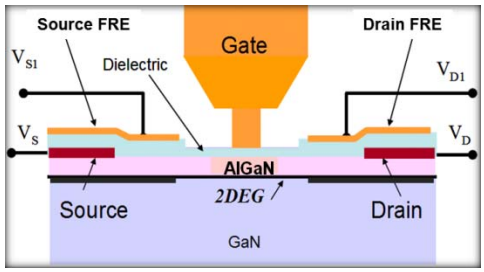

Fig. 4: Proposed deep submicron-gate HFET with FRE-elements controlling the source and drain access regions.

Trapped charge and related gate and drain large signal dispersion is a severe problem impeding the performance of III-Nitride and other compound semiconductor devices. Frequency-configurable electrode design can be employed to effectively remove the trapped carriers by discharging them using FRE-elements with carefully designed characteristic charge - discharge times. FRE-approach offers an unprecedented flexibility in discharging the trapped charge as the required elements with independently fine-tuned parameters can be located on the surface as well as being buried within the epitaxial structure.

The reliability of high-power devices is strongly correlated with the degree of the gate/drain lag and hence with the amount of trapped charge. Therefore, the proposed novel design will have a significant positive impact on the device reliability.

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DEMONSTRATION OF RTD OSCILLATIONS BEYOND TUNNEL-LIFETIME LIMIT

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ABSTRACT

Mm-wave oscillators are presented based on resonant-tunnelling diodes (RTDs) which are operated beyond their tunnel-lifetime limit. The tunnel lifetime of the electrons in the quantum well of an RTD is usually assumed to be imposing an inherent fundamental limitation on the operating frequencies of RTD [1]. While theoretical arguments against such an alleged fundamental limitation have already been shown [2-4], this paper demonstrates the first experimental verification for oscillations beyond the tunnel-lifetime limit.

1. INTRODUCTION

RTDs are actively studied for around four decades already [5, 6]. They are the simplest structures with resonant tunneling and therefore attractive for investigation of fundamental issues related to tunneling and resonant tunneling. Also, their I-V curve has a characteristic N-shape with a region of the negative differential conductance. This property is commonly used to compensate the attenuation of resonators and build oscillators.

Recently, an unexpected property of resonant-tunneling diodes has been discovered theoretically [3]. The tunnel lifetime (τ) of the resonant states in the quantum well is not necessarily a limitation for the maximum frequency. If the RTD is carefully designed, the negative differential conductance (NDC) – which is the key effect for oscillations – stays negative at frequencies beyond the reciprocal tunnel lifetime. This effect has been already demonstrated experimentally at 10 GHz [7] and should persist at higher frequencies according to the theory. Here, an experimental demonstration at 100 GHz is presented which deploys such a special RTD for the first time in an oscillator.

2. DESIGN

The collector of our RTDs is heavily doped. As it has been theoretically predicted [3, 4], it should be possible to achieve NDC at frequencies $\omega\tau>>1$ in such RTDs. The band profile of the designed RTDs is also optimised for fast electron transport in the collector: electrons are injected from the quantum well into the collector at sufficiently low energy, so that they can rapidly cross the depletion region on the collector side of the diode without scattering into higher L- and X-vales. Low bias of the current peak also guarantees low heating of the diode which is essential for continuous operation.

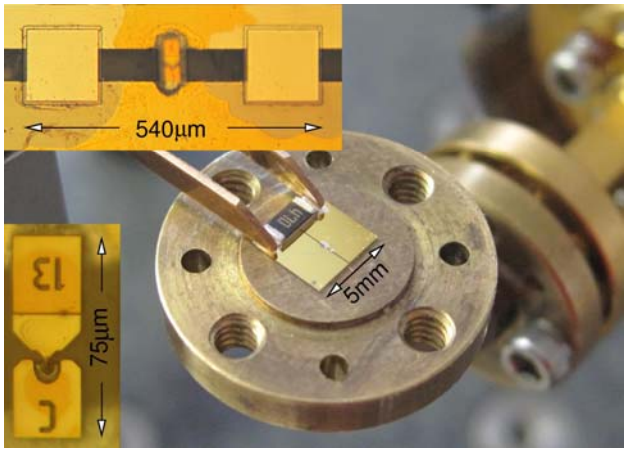

Fig. 1: An RTD (bottom left) is mounted into a 109 GHz slot antenna (top left) and the resulting oscillator chip is placed on the input waveguide of a spectrum analyser. The SMD resistor suppresses parasitic oscillations.

Two wafers were designed, which differ by the barrier thickness only. The RTD barriers are sandwiched by $In_{0.53}Ga_{0.47}As$ layers lattice matched to the InP substrate with an undoped spacer of ≈ 1 nm close to the barriers and the doping of 1.5×10^{18} cm^{-3} in the more distant layers including the collector. The AlAs barriers have a thickness of 2.7 nm in wafer W1 and 2.0 nm in wafer W2. The barriers were sandwiching a composite quantum well consisting of three layers $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}$ As with the thickness of (nominally) 1.2 nm each.

3. EXPERIMENT

A series of RTD oscillators has been fabricated with the fundamental frequencies in the range 33-150 GHz, which is chosen to meet the availability of accurate measurement equipment for precise analysis.

Here we report the highest value of the parameter $\omega\tau=3$ which has been measured at 109 GHz (wafer W1 with $\tau=4.4$ ps, details on calculation of τ are presented in [8]). All RTD oscillators reported till now had $\omega\tau<1$. The highest value of $\omega\tau$ reported in the past was $\omega\tau\sim0.7$ at 38 GHz [9], for THz RTDs the typical values of $\omega\tau$ are in the range 0.05-0.6.

For the time being, we have chosen slow RTDs with comparably thick barriers to elaborate accurate models

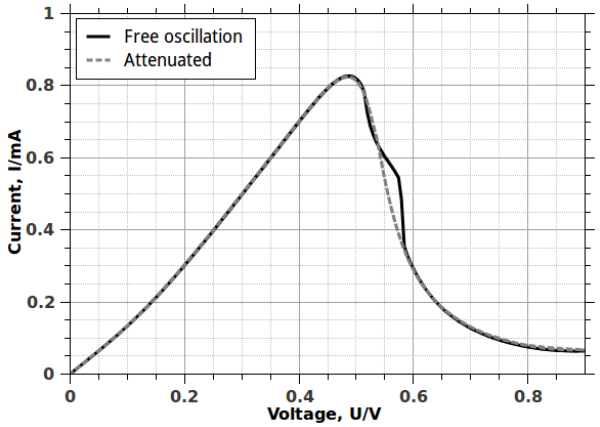

Fig. 2: IV curves for free oscillation (109 GHz) and with an attenuator to suppress oscillations for comparison.

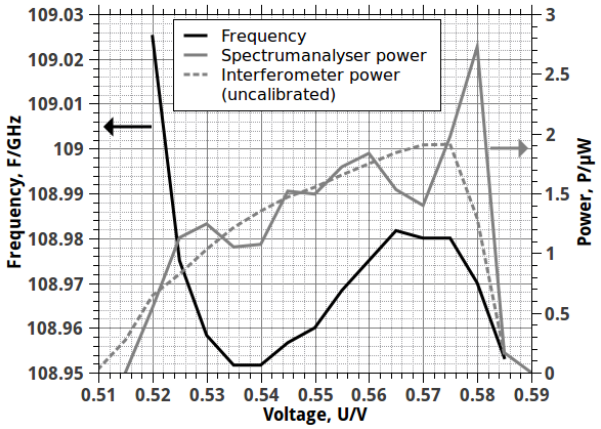

Fig. 3: Frequency and coupled power of the 109 GHz RTD oscillator. Power levels have been measured with a spectrum analyser and an interferometer for comparison.

and to avoid unnecessary excessive technological and measurement complications. Special care has been granted to the design of the antenna which serves the coupling of the RTD to free space and determines the resonance frequency in combination with the RTD. The antenna losses have been minimised by design and verified with measurements on scaled antenna models. A high Q-factor has been obtained and hence a large resonant impedance which is governed predominantly by the losses in the RTD and its interconnections. The oscillator chip consists of three parts: antenna, RTD and a resistor (which is connected in parallel to RTD to suppress the low-frequency oscillations). The slot antenna is formed by two metal half-plains deposited on top of 50 µm thick fused-silica substrate. Two metallization layers are needed to supply bias to the RTD. The metallization layers are overlapping in the regions of two capacitors. The metal layers are separated by ~600 nm of low-stress Si_3N_4 in the planar capacitors. The capacitors are seen as squares at the ends of the slot antenna in the upper inset in Fig. 1, and they are defining the length of the antenna slot. An RTD is soldered in the middle of the slot antenna. A discrete RTD chip is shown in the inset on the left-bottom side in Fig. 1. The RTDs are fabricated on a transferred membrane (several µm thin) substrate and they are contacted from the front and back sides. The use of a back-side contact allows us to decrease the parasitic resistance of the diode. The bias is supplied to the oscillator chip via the metal tips of the chip-holder, which are seen on the left of the photograph. The tips are holding the oscillator chip by the resistor, glued to the antenna.

4. RESULTS

The fabricated RTD oscillators have been characterized by IV curves first. If oscillations occur, the IV curves are altered, as shown in Fig. 2. By placing RF absorbing material close to the slot antenna, the losses significantly increase. The artificially introduced losses prevent oscillations, which enables a detailed analysis of the IV curves. Measurements have been carried out with a conventional w-band spectrum analyser and a dedicated Martin-Puplett interferometer for detailed characterisation. The coupling of the oscillator's output power to the waveguide of the spectrum analyser has been simulated to be around 30 %. Taking the coupling into account, the output power of the oscillator is around 8 µW. The obtained power and oscillation frequency are given in Fig 3.

5. CONCLUSION

We demonstrate the first experimental proof that operation of RTD oscillators in the regime $\omega\tau>1$ is possible. The measurements exhibit sound agreement with the underlying theory for power levels and IV curves.

ACKNOWLEDGEMENT

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FULL-SCALE NON-LINEAR ANALYSIS OF III-V NITRIDE BASED TRANSIT TIME DIODE FOR HIGH-POWER GENERATION IN THE TERAHERTZ REGIME

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ABSTRACT

A generalized technique based on self-consistent drift-diffusion model has been used for the large signal simulation of DDR IMPATT diode in the THz-region. The method, based on voltage-excitation, incorporates the effects of mobile space charge, diffusion and realistic temperature and field dependent material parameters. Simultaneous numerical solution of Poisson's equation, continuity equations and space charge equation is obtained in a suitably chosen number of space-steps and time-steps respectively. The results provide the electric-field and current density profiles in both space and time domain. The time evolution of electric field and carrier current density of the diode has also been obtained. A large signal efficiency of 6.6% and output power of 7W at around 1.0 THz have been obtained.

1. INTRODUCTION

IMPATT has emerged as the most powerful and efficient source at millimeter and sub-millimeter wave frequency bands. The authors have proposed a generalized and novel technique for large-signal simulation of DDR GaN IMPATTs. Large-signal analysis of IMPATT diodes and other negative resistance devices is based on two approaches. One of these is *self consistent analysis*, in which the voltage and current at the device terminal are related to each other through equations following the drift-diffusion model. The other approach is *idealized circuit analysis* in which the voltage waveform is taken as input and the current waveform is obtained from device equations. On the other hand, the current waveform may be taken as input and corresponding voltage waveform is obtained. Typically the waveform is chosen as a sinusoid of single frequency or the resultant of several sinusoids of arbitrary amplitudes and phases. The single frequency analysis is convenient because the results (impedance or admittance plots as a function of the frequency and amplitude) can be easily interpreted. In the present paper the authors have used a *voltage – excitation method*, in which a sinusoidal voltage is assumed to be applied across the device, the current response is calculated and then FOURIER analyzed. This method provides self-consistent numerical solution of the equations describing carrier transport, carrier generation and space charge. The authors have made the analysis more realistic by incorporating the realistic field dependence of carrier-ionization rates and drift velocities of electron-holes in GaN. The present method of large signal simulation is free from all assumptions and applicable to any IMPATT device structure with arbitrary doping profile and also for different frequency bands.

2. MODELING & SIMULATION

The electric field is considered in this study is in the following form:
$E = E_m + mE_m \sin(\omega t)$. The RF modulation m is varied from 20% to 70%, in order to study the effect of modulation on large-signal characteristics. The physical phenomena take place in the semiconductor bulk along the symmetry axis of the mesa structure of Impatt diodes. The fundamental device equations i.e., Poison's equation, current density equation and continuity equation involving mobile space-charge in the depletion layer are simultaneously solved under appropriate boundary conditions by using a double iterative field maximum computer method. The approach of *large signal simulation* is to obtain self-consistent numerical solutions for the equations describing carrier transport, carrier generation, and space charge balance in a one dimensional semiconductor structure [1-2]. The solution describes the evolution in time of the diode and its associated resonant circuit. Basically the program solves the following problem at various instances of time during a cycle of oscillation. Given, the instantaneous distribution of the hole and electron concentration and terminal boundary conditions, it will be possible to know the movement of carriers with respect to time. Given the carrier, the program determines the electric field by Poisson's equation and knowing the electric field and carrier concentration, it obtains the instantaneous hole and electron particle currents (including the dependence of carrier mobilities upon impurity concentration and electric field strength). From the particle current and the generation rate including generation and recombination by field dependent impact ionization and carrier concentration dependent single level recombination centres, it obtains the time derivate of the carrier concentrations from the continuity equations. From the time derivative of the carrier concentration, the program computes the carrier distribution and instant in time later, and repeats the cycle.

The total terminal current (i.e. the external current) is given by, $I(t) = C_d \; d(-V)/dt + I_e(t)$

Where, C_d is the depletion region capacitance of the diode, V is the AC terminal voltage and I_e is the terminal current induced by the transport of carriers through the diode (Fig. below).

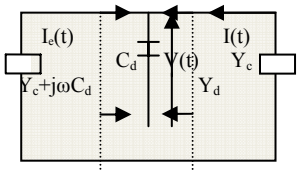

Fig.1: Terminal voltage and current for an IMPATT diode showing the separation of the depletion region capacitance C_d from the diode admittance Y_d. Y_c is the circuit admittance including the diode package.

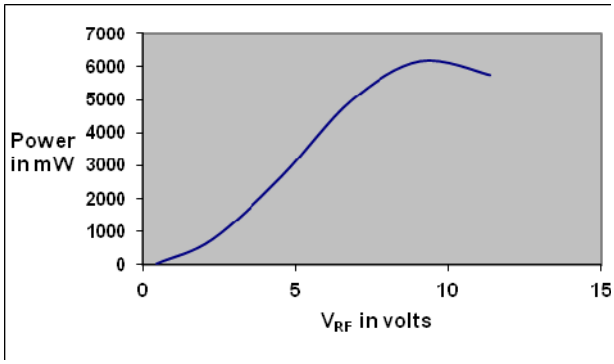

Fig. 2: Large signal power output of GaN THz IMPATT

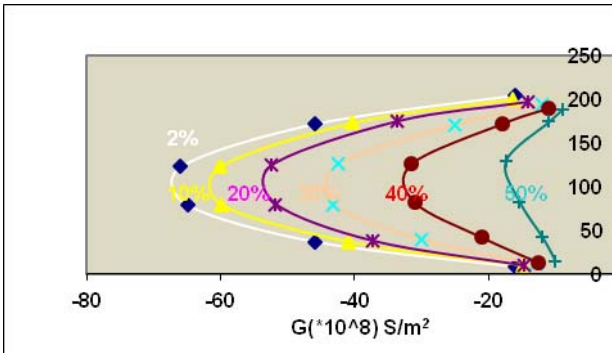

Fig.. 3: Large signal admittance plots of GaN THz IMPATT

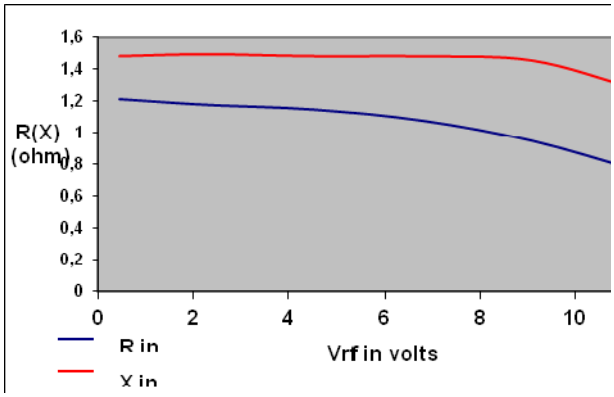

Fig.4: Large signal impedance plots of GaN THz IMPATT

The diode admittance (including the depletion region capacitance (C_d) at the oscillation frequency ω is given by the fundamental frequency components of current and voltage by,

$Y_d = j\omega C_d - \frac{I_{e1}(\omega)}{V_1(\omega)}$, Finally the expression governing the terminal voltage V(t) is given as, $V(t) = \{A_0 l_d / \varepsilon\omega A_r\} * \cos\omega(t + \tau_d/2) -$ $[2x\, A_0 l_d\, x \sin(\omega\tau_d/2) x \cos\omega t\, A_0\, \omega \cos\omega(t + \tau_d/2) / (\omega^2 \tau_d\, \varepsilon\, A_r)] - \{\tau_a\, E_c\, l_d/2*m\} * A_0\, \omega \cos\omega(t + \tau_d/2) / I_{dc} + A_0 \sin\omega(t + \tau_d/2)$,

The diode admittance is found to be,

$Y_d = j\omega C_d + [j\omega C_d * A_0 * I_{RF} * \exp(-j\omega\tau_d/2)] / [A_0^2 - A_0^2 [\sin(\omega\tau_d/2)/ \omega\tau_d/2] * \exp(-j\omega\tau_d/2) - 2*I_{dc}*\omega^2/ \omega_a^2 [I_{dc} - (I_{dc}^2 - A_0^2)^{1/2}]]$

The symbols have their usual significance. A generalized simulation scheme is developed to produce the admittance plots for different modulation factor as shown in this paper. The accuracy of the developed simulator is increased by considering a space division of 500 steps and time scale is varied from 5-20. Large signal power, negative resistances are obtained accordingly.

3. RESULTS AND DISCUSSIONS

The device characteristics are studied at different modulations. It is observed that with increasing modulation, efficiency degrades. However the power output initially increases up to 50% modulation and then on increasing modulation further, RF power degrades (Figure 2). Similar phenomenon is observed in case of admittance characteristics. It is also found that the increasing modulation degrades the conductance and as a result the Q-factor degrades. In Fig.3 the admittance characteristics shows that the negative conductance decreases from its peak value with increasing modulation ,whereas Figure 4 show the variation in cases of negative resistance and reactance.

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GRAPHENE DEVICES FOR MICROWAVES AND TERAHERTZ APPLICATIONS

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ABSTRACT

The most studied microwave graphene device is the transistor, which in few years has attained the cutoff frequency of 300 GHz and is expected to reach the THz region within few years. We review briefly the graphene FET devices and focus on other devices and concepts such as graphene coplanar waveguides, graphene multiplication, NEMS devices, antennas and graphene sensors. In this way, a broader image on graphene applications at high frequencies emerges.

1. INTRODUCTION

Graphene is a monoatomic layer material with a thickness of only 0.34 nm composed of carbon atoms in the sp^2 hybridization state. In graphene, each carbon atom is covalently bonded to three others, so that the graphene lattice is a honeycomb composed of two interpenetrating triangular sublattices. Graphene is the first 2D material ever found and is the orgin of many carbon-based materials such as high order pyrolytic graphite, formed by billions of stacked sheets of graphene, and carbon nanotubes, which consist of a single or multiple rolled-up graphene sheets [1].

Graphene is a weird material because it cannot exist in a free-standing form, since it breaks due to its surface energy. On the contrary, if graphene is deposited on a surface, such as SiO_2 deposited on a Si substrate, graphene is a two dimensional atomic layer. This fact explains the graphene discovery by mechanically exfoliating of high ordered pyrolytic graphite (HOPG) on a 300 nm SiO_2 layer deposited on a Si substrate [2]. The texturing control of the graphene substrate, i.e. its roughness, is a key parameter and allows the design of graphene-based devices creating local strain through the deformation of graphene [3]. The roughness has a key role also in the electrical performances of graphene. For example, on SiO_2 substrates, mobilities higher than 10 000 cm^2/Vs are difficult to obtain due to impurities and various scattering mechanisms. On the other hand, the graphene suspended membrane displays much higher mobilities, but it is fragile and mechanical instable. The hexagonal boron nitride substrate, which matches the graphene lattice, allows mobilities higher than 100 000 cm^2/s [4] and mean-free carrier paths of 1 μm at the room temperature [5].

The band structure of graphene is linear near the K and K' points in the reciprocal lattice: $E = \pm\hbar|\mathbf{k}|v_F$ where $\mathbf{k} = \mathbf{i}k_x + \mathbf{j}k_y$ is the wavevector measured from K or K', v_F is the Fermi velocity of 10^6 m/s, and the positive (negative) sign is assigned to electrons (holes). This linear dispersion relation is formed from two cones, as shown in Fig. 1. We observe that graphene is a zero-energy-gap semiconductor since the valence and conduction bands touch at only one point, termed the Dirac point.

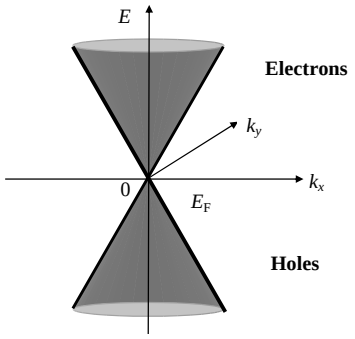


Fig. 1: Graphene dispersion relation.

In graphene, the linear dispersion means that the effective mass of charge carriers is zero, the ballistic transport of carriers taking place at room temperature along 0.2-1 μm, depending on the graphene substrate. The ballistic transport is the key concept of high-frequency devices beyond 100 GHz, since the cut off frequency of these devices is proportional to the traversal time of carriers between the contacts.

Graphene, despite its extreme thickness of one atom (graphene monolayer), two atoms (graphene bilayer), or few atoms (graphene multilayer) in thickness, is still visible with a simple optical microscope with a filter. Figure 2 illustrates an optical image of a graphene monolayer and bilayer (by courtesy of Graphene Industries). More details are found in references [6-8]. Also, Raman spectroscopy is able to identify the type of graphene and its thickness [9,10]. Graphene is the

strongest material, with an elastic stiffness of 340 N/m and a Young modulus of 1.5 TPa [11] and can be bent by 15-20%, making it very attractive for flexible electronics and NEMS. Graphene has many other interesting electrical, mechanical, and optical properties (very high mobility, Klein tunneling or Hall effect, etc.) which are the origin of its attribute as "wonder material" [12].

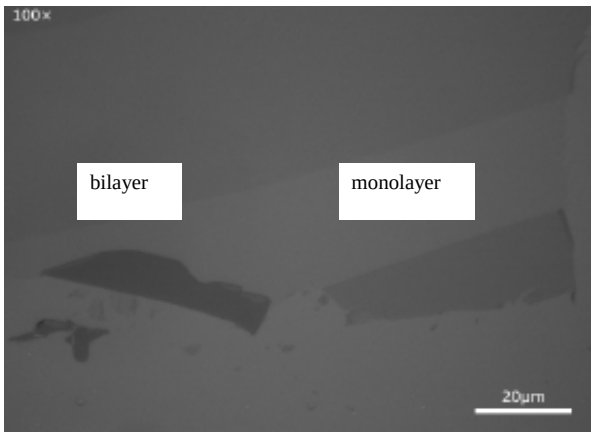


Fig. 2: Optical image of graphene monolayer and bilayer.

Graphene is produced at the wafer scale and even larger, and many recent reviews explain in detail the graphene growth techniques [13,14]. The most promising method to grow graphene is CVD, the graphene films being fabricated by roll-to-roll techniques up to 30-inch on flexible copper substrates, with direct applications in flexible electronics where these films are used as transparent electrodes or displays [15]. Irrespective of the growth method, the graphene obtained via these deposition methods displays modest performances compared to the mechanical exfoliated graphene obtained from HOPG, so still growth methods are not able to reproduce what the nature has created. Graphene is compatible with standard fabrication techniques used for semiconductor devices.

2. MICROWAVE AND MILLIMETERWAVE DEVICES BASED ON GRAPHENE

Due to its impressive properties, graphene devices are the most researched ones in the area of nanoelectronics for transistors [16], spin valve devices [17], photodetectors [18], single-electron transistors [19], and solar cells [20]. However, only few works have been reported up to now in the area of microwave applications. There are many reasons for this moderate interest. First, the microwave devices and circuits are fabricated up to 125 GHz using GaAs, SiGe, InP, SiGe or high-resistivity Si, with established technologies implemented in semiconductor fabrication plants. Then, nanomaterials such as nanoparticles, nanowires, and carbon nanotubes intensively studied in nanoelectronics, nanomedicine, or biology display very large impedances (typically greater than 10 kΩ), which simply do not match with the standard 50 Ω impedance. In the case of carbon nanotubes, many nanotubes are arranged in parallel to get the 50 Ω impedance [21] and transistors up to 80 GHz were fabricated [22]. Graphene microwave field-effect transistors (FETs) are the most researched graphene devices with a very high impact for the microwave domain. In few years the cut-off of graphene FETs has increased from a few GHz to 100 GHz [23] due to much better fabrication technologies, allowing a decrease in the gate length and the use of dielectrics which, when deposited on graphene, do not damage it dramatically. An updated review about graphene transistors is [16]. The cutoff frequencies of the graphene FETs increases very rapidly, and at the end of the last year a graphene transistor having a nanowire (CO_2Si-Al_2O_3 core-shell nanowire) as a gate and a cut-off frequency exceeding 300 GHz [24] was reported. However, the extrinsic cutoff frequencies of graphene FETs do not exceed 15 GHz, due the large parasitic capacitances.

Regarding microwave and millimeterwave applications, the first concern is if graphene is able to reach the desired 50 Ω impedance. We have recently fabricated and characterized a coplanar line (CPW) deposited on graphene, we have measured its properties up to 65 GHz, and finally we have determined the equivalent circuit of the CPW [25], having a resistive part of the impedance of nearly 50 Ω. This important result was used further by a group at Princeton University to measure the quantum oscillations in graphene within the microwave range [26], demonstrating the validity of our concept. A blowup of the CPW graphene device is displayed in Fig. 3, where the relevant dimensions are indicated in the SEM photo. Beyond the graphene region we have patterned a metallic CPW to fit the dimensions of the probe tip pitch, of 150 µm.

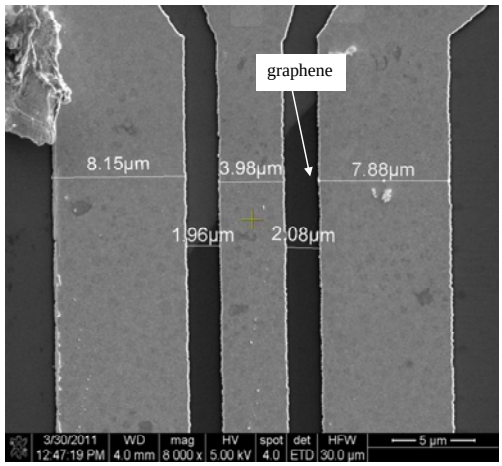


Fig. 3: Detail of the CPW graphene device.

The S-parameter measurements up to 110 GHz are displayed in Fig. 4. We can see from Fig. 4 that the S parameters depend on the dc voltage applied on the CPW. The equivalent circuit is a parallel RC circuit. A good agreement between the simulated and experimental results were found for the Si permittivity of ε_r = 11.9, a conductivity of 0.05 S/m and a loss tangent of 0.05. The simulations have shown that graphene can be modeled as a parallel lumped circuit connected as an internal port

with the CPW electromagnetic model. The resistance is varied in the range 50- 90 Ω for biases between -6 V and 6 V, while the capacitance remains almost constant, around 60 fF.

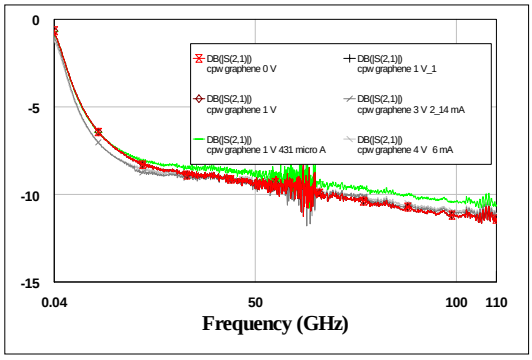
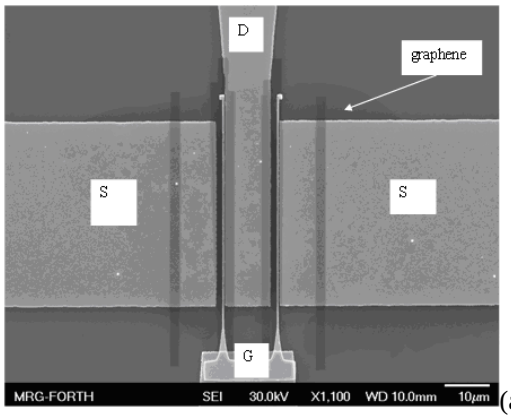
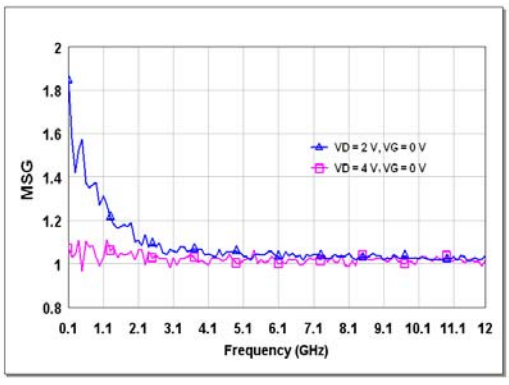


Fig. 4: The broadband transmission $|S_{21}|$ of the CPW graphene up to 110 GHz.

We have fabricated an RF graphene transistor [27] in a double-gate configuration placed over graphene, which has the role of the channel between the source (S) and drain (D) electrodes (see Fig. 5a).



(a)



(b)

Fig. 5: (a) The graphene FET transistor and (b) its maximum stable gain at the Dirac point and far from it.

The gate electrodes are separated from graphene by a thin PMMA layer of 200 nm thickness, which does not destroy the graphene lattice. The substrate is a 300 nm SiO_2 layer grown on high-resistivity Si and the graphene was deposited by Graphene Industries. The dimensions of the graphene FET are: gate length L_g = 200 nm, source-drain distance L = 2 μm and source/drain width W = 40 μm. We have measured a maximum stable gain greater than 1 up to 5 GHz. It is noteworthy that far from the Dirac point the graphene FET behaves as an active device, i.e. amplifies the microwave signals, while at the Dirac point the transistor becomes passive, its amplification being suppressed due to carrier recombination (Fig. 5b).

3. TERAHERTZ DEVICES BASED ON GRAPHENE

Similar to the famous Moore law, the Edholm law states that the need for higher bandwidths in wireless communications has doubled every 18 months. Now, in wireless LANs the carrier frequencies are around 5 GHz and the data rates reach 110-200 Mb/s. However, according to Edholm law, wireless data rates around 5 Gb/s will be required in 8-10 years from now. This means that the carrier frequencies for wireless communications should be higher than 100 GHz, thus reaching the terahertz domain, which is located in the bandwidth 0.1-10 THz [28]. However, in this bandwidth the devices and circuits able to form a wireless link at room temperature are very scarce. There were many efforts to break the 100 GHz barrier involving semiconductor heterostructures fabricated with the most advanced techniques, but there are very few semiconducting devices able to work beyond 125 GHz. This limitation is due to the relative high scattering time and the relative low mobilities encountered in all semiconductors at room temperature. Graphene has no such limitations. There are still no devices fabricated on graphene working at THz frequencies, but some steps are done in this direction. For example, the graphene absorption spectra were measured from the THz region up to visible [29], and the generation of subpicosecond THz pulses was measured in HOPG when illuminated with a fs laser [30]. The authors noted than even the graphite tip of a pencil is able to emit THz radiation! This is due to the strong nonlinearities encountered in graphite, and in graphene in particular, at THz frequencies. We have proposed also several devices able to generate THz frequencies such as: Bloch oscillators [31], ultrafast Schottky diodes [32], and THz antennas [33] based on graphene.

The Schottky diode is the key component in THz electronics for generation by multiplication or for detection purposes. A graphene-based ballistic Schottky diode is able to rectify an incident signal due to an oblique gate positioned between the two terminals of the device (see Fig. 6). The operating point of the diode can be prescribed by the applied gate voltage, while the current-voltage dependence of the device can be changed by varying the inclination angle of the gate. The ideality factor of the graphene-based diode can take values higher or lower than 1 by modifying this inclination angle.

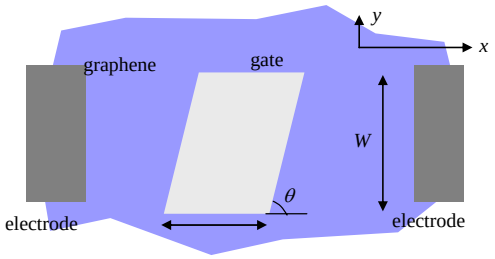


Fig. 6: Graphene-based Schottky ballistic diode with an oblique gate.

The rectifying properties of the graphene diode are tunable, in deep contrast with semiconductor-based diodes (see Ref. 33 for more details). Another type of Schottky on graphene, where Ti was used as a Schottky contact and Pt for the ohmic contact, is displayed in Fig. 7. The measurements of this diode are performed during the writing of this manuscript.

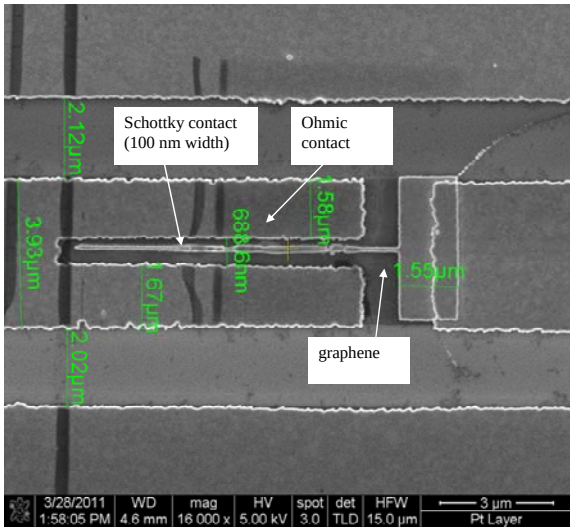


Fig. 7: Another graphene-based Schottky diode.

4. CONCLUSIONS

The microwave, millimeterwave and THz applications of graphene are of paramount importance in the development of microwaves, photonics, THz electronics, and other areas. These applications exploit the unique features of charge carrier transport in graphene. The research on graphene-based high-frequency devices is fast increasing.

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Session 3 :

Graphene and carbon nanostructures

Chair : Prof. Luigi Colombo

Monday May 30, 14:30 - 16:00

FAST GRAPHENE ELECTRONICS AND PHOTONICS

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ABSTRACT

We present experimental results on high frequency field-effect transistors and fast photodetectors utilizing wafer-scale graphene grown epitaxially on silicon carbide, or by chemical vapor deposition on copper.

1. INTRODUCTION

Graphene is a 2D electron system comprised of a single layer of carbon atoms arranged in a hexagonal honeycomb lattice. It is a zero-gap semiconductor with linear dispersion, vanishing rest mass, large carrier mobilities, and strong and nearly constant optical absorption over a wide wavelength range (from far IR to almost the ultraviolet) [1]. These characteristics make graphene ideally suited for fast analogue electronics and optoelectronics [2]. Here, we demonstrate and discuss applications of graphene in radio-frequency (RF) transistors (>100GHz) for applications in communications. We also describe a new principle for a graphene photodetector and demonstrate devices with >50 GHz photoresponse, which are then utilized to faithfully detect optical data streams at 10 Git/s. Finally, we demonstrate the opening of a field-tunable electronic band gap in bilayer graphene at room temperature.

2. RF GRAPHENE TRANSISTORS

Technological applications of graphene in electronics require large (wafer) scale, well characterized graphene. In our work we employ two types of graphene synthesis. One involves epitaxial graphene produced by thermal decomposition of 4H(0001) SiC wafers to form a graphene-terminated wafer surface [3]. The other is based on the catalytic decomposition of hydrocarbons (e.g. CH_4 or C_2H_4) on copper [4]. In order to fabricate transistors, the continuous graphene layer is patterned by oxygen plasma etching and source/drain electrodes are deposited by thermal metal (Pd/Au) evaporation. Top-gate stacks are then formed by either depositing an organic seed layer (NFC polymer) followed by HfO_2 or Al_2O_3 atomic layer deposition (ALD) [5], or by plasma-enhanced chemical vapor deposition (PECVD) of a thin silicon nitride film [6], followed by gate metal deposition. Figure 1 (top) shows a 2-inch graphene wafer from SiC with arrays of RF graphene field-effect transistors (FETs) fabricated using e-beam lithography [7]. Fig. 1 (bottom) shows an AFM image of the graphene surface. Terraces and steps are clearly seen.

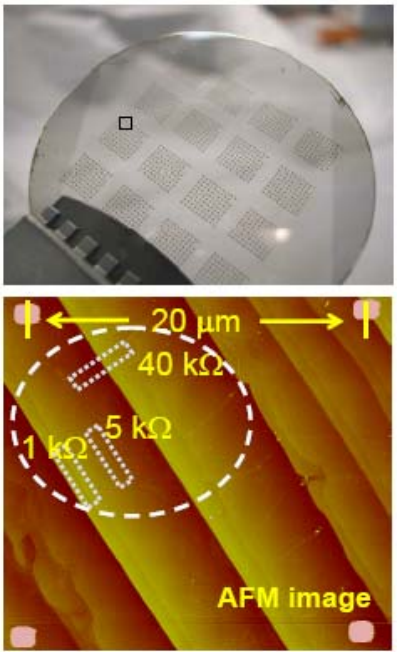

Fig. 1: Top: Graphene formed on a SiC wafer and array of graphene transistors formed on it by e-beam lithography. Bottom: AFM image of a typical graphene surface formed from the Si-face of SiC.

As expected, the detailed topography of the graphene influences its transport properties and this is demonstrated in Fig. 1(bottom) by the different resistances measured by fabricating otherwise identical devices in different parts of the surface. The RF performance of the graphene FETs is determined by measuring their S-parameters.

In Fig. 2 (top) we show the structure of one of these RF transistors. In Fig. 2 (middle) we give the current gain (h21) vs. frequency (f) of two such devices with gate lengths of 550 nm and 240 nm. These are fabricated, without pre-selection of the sites, on a monolayer epitaxial graphene sample with a carrier (hole) mobility of about 1,500 $cm^2/V{\cdot}s$. The 550nm device has a cut-off frequency (f_T) of 53 GHz, while in the scaled 240 nm device the f_T increases to 100 GHz. [7]. This is a very encouraging result, given the large gate length (corresponding Si-based transistors give a f_T of about 40 GHz) [8], and the rather modest mobility of the graphene used. Fig. 2 (bottom) shows again an Lg=240 nm device, but this time care was taken to fabricate the device on a single graphene terrace and to minimize the access

resistance in the device. Here the cut-off frequency is increased to 230 GHz. It is clear that graphene is capable of achieving very high frequencies upon improving the quality of graphene (mobility), and controlling its topography and device structure.

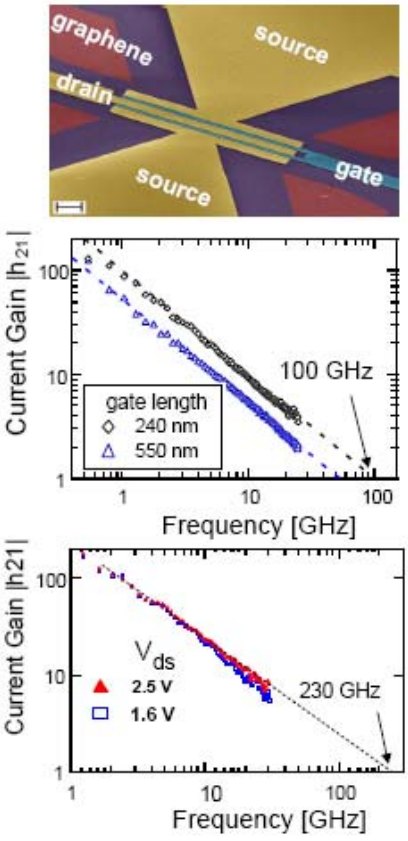

Fig. 2: Top: The structure of one of our RF graphene transistors. Middle: Current gain (h21) vs. frequency of two graphene FETs with gate lengths of 550 and 240 nm, respectively, fabricated on a SiC-derived monolayer graphene. Bottom: Current gain vs. frequency for another 240 nm FET fabricated on a single graphene terrace of the same sample.

While the highest mobilities of synthetic graphene have been obtained with the SiC method, there are two disadvantages with this technique. One involves the difficulty of controlling the number of graphene layers produced, the other is the high price and limited size of available SiC wafers. More recently, CVD growth of graphene on copper films [4] appears to eliminate these problems, although the mobilities demonstrated so far are not as high. We have tested this approach and have fabricated transistors on CVD graphene and scaled them down to gate lengths as short as 40 nm [9]. In Fig. 3 we present results from such a device. The graphene mobility was only about 900 $cm^2/V{\cdot}s$, but we were able to obtain a f_T of 155 GHz, the highest observed so far for CVD graphene. Moreover, we performed studies of the FR performance of these devices at both room temperature and at liquid helium temperature and observed no degradation of the performance, i.e. no carrier freeze-out was observed in the graphene devices, as shown in Fig. 3 [9].

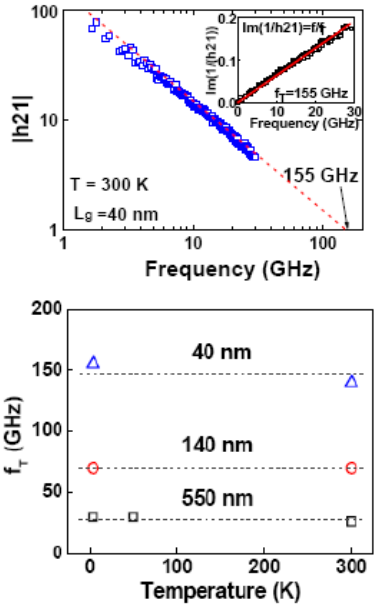

Fig. 3: Top: Current gain curve for an Lg= 40 nm CVD transistor device. A cut-off frequency of 155 GHz at 300K is deduced by two independent methods. Bottom: Cut-off frequency (f_T) as a function of temperature.

3. FAST GRAPHENE PHOTODETECTORS

Free-standing graphene absorbs about 2.3% of the incident light, independent of the wavelength over a very wide wavelength range spanning the visible and infrared ranges [10]. The wide range and constant absorption of graphene make it a desirable material for a 'universal' photodetector [2]. In addition, the fast carrier transport and the fact that, unlike in conventional semiconductors (e.g III-V's), both components of the photo-excited e-h pair have high mobilities, suggest a very fast response of such a detector. However, graphene is a zero gap semiconductor. If a voltage is applied across it, a large dark current develops, which would also lead to large shot-noise. For this reason, we focused on the properties of graphene-metal contacts. In contacts that preserve the structural integrity of graphene under the metal, such as Pd-graphene contacts, there is charge-transfer between the two systems and the graphene becomes doped. This leads to a 'band-bending' in the vicinity of the contacts [11,12]. As a result, a built-in electric field is generated in the vicinity of the contact. Photoexcitation near the contact generates e-h pairs that can be separated by the built-in field to produce a net photocurrent. [13-15]. A schematic illustration of these effects is shown in Fig. 6 (top). We note that the field direction at the source and drain contacts is opposite. Therefore, in a symmetric device, simultaneous illumination of both contacts leads to equal but opposite polarity currents and no net photocurrent.

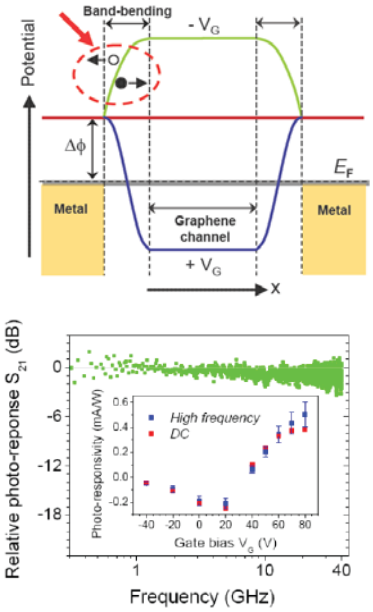

Fig. 4: Top: Schematic potential energy diagram of the bending of the graphene bands near the metal contacts and the separation of photo-excited electron-hole pairs. Bottom: Relative photoresponse (S_{21}) of a two-electrode graphene photodetector as a function of the modulation frequency of the 1550 nm light illuminating one contact. Inset: Comparison of the RF and DC photoresponses of this device.

Figure 4 (bottom) shows the frequency dependence of the photoresponse of a graphene photodetector for illumination of one contact with 1.55 micrometer light [16]. A nearly flat photoresponse was observed up to the frequency limit of the measurement system (40 GHz). It is likely that the photoresponse of such a photodetector would be much faster, limited only by RC considerations in the region of about 0.5 THz. At high light intensities and higher photon energies, thermalization will lead to the generation of a thermovoltage, which will act at longer time scales.

Improvements to the simple photodetector described above involve generating a device that utilizes the full surface of graphene for photodetection and an increased value of the photoresponse. Such a structure is shown in Fig. 5 [17]. It involves multiple interdigitated electrodes made of two different metals: one with a high work function, in this case Pd, and one with a low, in this case Ti. At appropriate back-gate biases, the two different work-functions and resulting asymmetric band-bendings generate a sloping potential along the graphene channel that allows photodetection over the entire device [17]. Furthermore, the multi-finger electrodes increase drastically the photoresponse [17]. This type of device was implemented (see Fig. 5) to reliably detect optical data streams of 1.55 μm light modulated at a rate of 10 GBit/s (maximum capability of the measurement system) without an applied source-drain bias [16]. Error-free detection at this rate was verified by the open eye measurement shown in the bottom of Fig. 5. Further enhancement in the photoresponse of the graphene photodetectors can be achieved by coupling to surface plasmons of the substrate or even of the graphene itself.

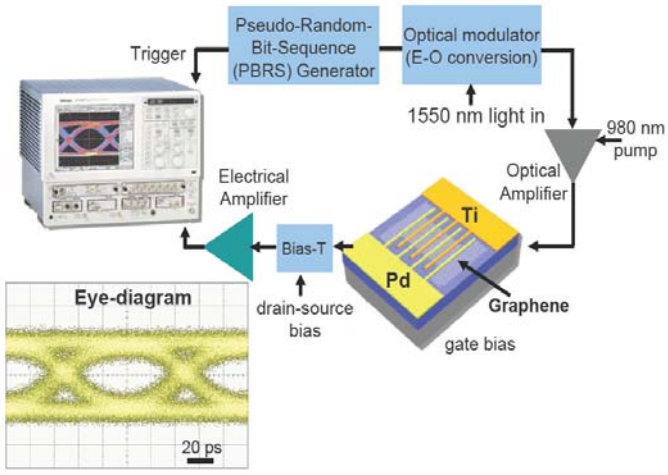

Fig. 5: Setup for the measurement of optical data streams at 10 Gbit/s using the multi-finger, two-different metal graphene photodetector. Bottom left: Open eye test indicating error-free detection of the optical data.

BAND-GAP IN BILAYER GRAPHENE

Monolayer graphene is a zero band-gap material with many possibilities for applications. However, if it were possible to open a band-gap many more opportunities would become available. The situation is simpler in AB bilayer graphene, of which, although also a zero-gap material, theory predicts [18] that a perpendicular electric field would break the symmetry and open a gap. However, while optically such a gap opening was indeed observed [19, 20], defects and defect-mediated transport precluded the observation of a substantial gap in electrical measurements.

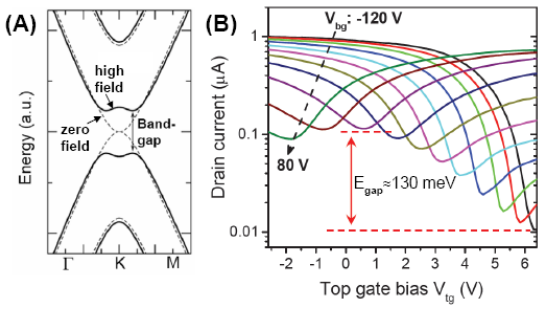

Fig. 6: (A) Schematic illustration of band-gap opening in bi-layer graphene by a perpendicular electric field. The dashed line denotes the potential with no applied field, while the solid line the potential with the field. (B) Drain current as a function of top gate bias of the double-gated bilayer graphene FET at room temperature. The back-gate bias, V_{bg}, is varied from -120 to 80V at steps of 20V.

In our work, we used a double-gated device and a thin seed layer polymer film cover of graphene to reduce the scattering by charges in the high-k dielectric gate oxide (HfO_2). As is shown in Fig. 6, we were able to produce transistors with a high current on/off ratio of ~100 and a field-tunable band-gap of ~130 meV at room temperature [21].

ACKNOWLEDGEMENTS

I would like to acknowledge my coworkers in the work described in this talk, particularly Yu-Ming Lin, Fengnian Xia, Yanqing Wu, Damon Farmer, Thomas Mueller, Christos Dimitrakopoulos and Ageeth Bol. This work was supported by DARPA under contract FA8650-08-C-7838 (CERA program). The views, opinions and findings contained in this abstract are those of the author and should not be interpreted as representing the official views or policies, either expressed or implied, of DARPA or the US Department of Defense.

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EPITAXIAL GRAPHENE ON OFF-AXIS 4H-SiC (0001): STUDY OF THE GROWTH MECHANISMS AND NANO/MICRO-SCALE ELECTRICAL CHARACTERIZATION

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ABSTRACT

The epitaxial growth of graphene on the Si face of off-axis 4H-SiC by high temperature (1600 – 2000 °C) thermal treatments in Ar was investigated. The electronic transport properties (mobility) of the grown layers have been probed both on micrometer scale, using standard test structures (van der Pauw, transmission line model, field effect transistors) and locally, on submicrometer scale, by scanning probe microscopy. The latter approach provided informations on the lateral homogeneity of the transport properties.

1. INTRODUCTION

Controlled graphitization of hexagonal SiC by high temperature thermal processes represents the most promising synthesis method of graphene for electronics applications, because graphene is directly obtained on a semiconductor/semi-insulating substrate without any need of transfer [1,2]. Graphene growth during annealing of SiC relies on the interplay of two mechanisms: (i) the preferential Si sublimation from SiC surface, which leaves an excess of C atoms, and (ii) the surface diffusion of these C atoms and their reorganization in the 2D graphene lattice structure. Both mechanisms depend on the annealing conditions (temperature T_{gr}, ramp rate, pressure in the chamber) and on the properties of SiC surface, e.g. the termination (Si or C –face) and the miscut angle. Epitaxial graphene (EG) growth starts from the kinks of the terraces on the SiC surface, and a higher growth rate is expected on off-axis SiC than on on-axis.
So far, most of the studies on have been carried out on on-axis semi-insulating hexagonal SiC [2], because it is easier to control the growth of single layers of graphene. However, off-axis 4H-SiC (0001) substrates with lowly doped epitaxial layers are the standard platform of current SiC technology and are available as (relatively) low cost large wafers of very high crystalline quality.
In this paper we investigated of the growth mechanisms and the electronic properties of EG on 4H-SiC (0001) off-axis, also in the perspective of a future integration of graphene electronics with SiC technology.

2. GRAPHENE GROWTH

The SiC substrates used for graphene growth were lowly doped (~10^{14} cm^{-3}) epi-layers on top of highly doped, 8° off-axis 4H-SiC(0001). Growth was carried out in Ar in a commercial furnace by Centrotherm thermal solutions GmbH + Co. KG at temperatures T_{gr} from 1600 to 1700 °C, or in an inductively heated reactor at T_{gr}=2000 °C.

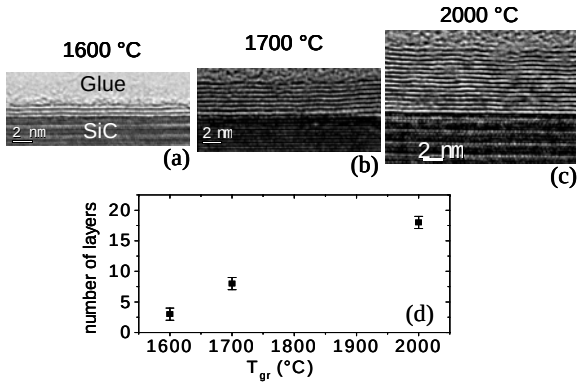

Fig. 1: High resolution transmission electron microscopy of graphene layers grown on 4H-SiC (0001), 8° off, at different temperatures: 1600 °C (a), 1700°C (b) and 2000 °C (c). Number of grown graphene layers as a function of the growth temperature (d).

For each growth temperature, the number of graphene layers (N_{gr}) was determined locally by high resolution transmission electron microscopy (HRTEM) and, on several sample positions, by atomic force microscopy (AFM) measuring the depth of selectively etched trenches (by O_2 plasma treatments) in graphene. Fig.1(a), (b) and (c) show HRTEM images of EG grown at 1600, 1700 and 2000 °C, respectively. N_{gr} is found to increase almost linearly as a function of the growth temperature in the considered temperature range (see Fig.1(c)). The few layers of graphene (FLG) are found to cover in conformal way the terraces of the SiC surface [3].

3. ELECTRICAL CHARACTERIZATION

The EG sheet resistance R_{sh} as well as the specific contact resistance ρ_c of contacts on EG were measured using Van der Pauw (vdP) and transmission line model (TLM) test structures, defined by electron beam or laser lithography, combined to O_2 plasma etching (for device lateral isolation), metal deposition and lift-off (for contacts). As an example, R_{sh}=700±10 Ω/sq and $\rho_c \approx 7\times10^{-5}$ Ω×cm^2 were obtained for EG grown at 1600 °C.

Carrier mobility in EG was measured using top gated field effect transistors (FETs) with different channel geometries, i.e. length L_G and width W. In particular, channel mobility in long-channel FETs are especially interesting, being strongly affected from lateral inhomogeneities in the electron mean free path associated to the inhomogeneous defects distribution in EG.

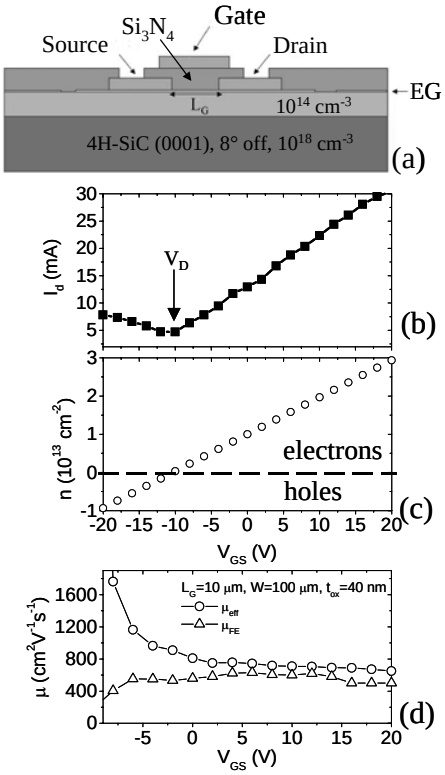

Fig. 2: Schematic of the cross section of a field effect device fabricated on epitaxial graphene, using 40 nm Si_3N_4 as gate dielectric (a). I_D-V_{GS} characteristics of the transistor (b). Carrier density in the EG layer as a function of V_{GS} (c). Effective mobility μ_{eff} and field effect mobility μ_{FE} vs V_{GS} (d).

PECVD deposited Si_3N_4 was used as gate dielectric and showed excellent coverage on EG, without any need of surface functionalization. Si_3N_4 deposition caused only a small (~10%) increase in the R_{sh} in EG, as deduced from measurements on vdP and TLM structures fabricated after dielectric deposition.

A schematic of the cross-section of a FET on EG grown at 1600 °C, with 40 nm thick Si_3N_4 gate dielectric, L_G=10 μm and W=100 μm is shown in Fig.2(a). The drain current I_D vs gate bias V_{GS} characteristic in Fig.2(b) exhibits ambipolar behaviour, with the minimum conductivity point at $V_D \approx$-10 V. This means that EG is highly n-type doped ($n \approx 10^{13}$ cm^{-2}) at V_{GS}=0 V (Fig.2(c)).

The extracted effective mobility μ_{eff} and the field effect mobility μ_{FE} in the electron conduction branch is reported in Fig.2(d).

The mobility values extracted from electrical measurements on these devices represent average values on micrometer areas and are the result of the combination of different scattering sources inhomogeneously distributed on EG.

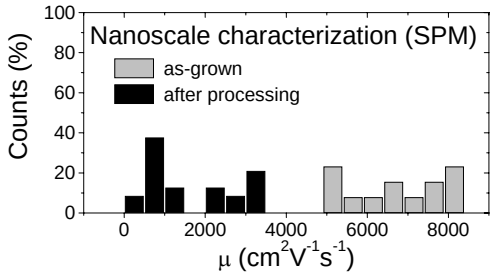

Fig. 3: Histograms of the locally measured carrier mobility values on 1μm×1μm area in as-grown EG and after processing.

To get a deeper understanding on the lateral homogeneity of the carrier mobility, local measurements of the electron mean free path in EG were carried out by a recently demonstrated scanning probe microscopy (SPM) method [4]. Assuming an average carrier concentration $n \approx 10^{13}$ cm^{-2}, the distribution of the carrier mobility values probed on 1μm×1μm area in EG is obtained. The strength of this method was to get access also to local μ_{local} values also in as-grown EG, without any need of device structures. The comparison of the histograms of μ_{local} both in as-grown EG and after device processing is reported in Fig.3. Broad distributions of μ_{local} values are obtained in both cases, but a significant degradation of the transport properties can be observed after processing and is probably associated to EG surface contamination.

It is worth comparing the average μ extracted from long-channel FETs with this distribution, to understand how μ_{local} combine to yield the macroscopic μ. Although this subject deserves further modelling, it can be observed that the lower μ_{local} values in the histogram have a stronger weight in the determination of the average μ between source and drain in a macroscopic FET.

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COERENT ELECTRON TRANSPORT IN QUASI 1D C-BASED SYSTEMS

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ABSTRACT

We discuss the methodology for studying coherent electron transport properties of non-ideal quasi-one-dimensional carbon-based systems. Results are based on the implementation of Schroedinger/Poisson scheme. Attention is paid on the role of modifications of the structural and electronic symmetry. Particular focus will be given to graphene based system showing sp^3 bonding due to H chemi-absorption. The objective is to elucidate the potentiality as well as the possible drawbacks of future all-carbon-based electronics.

1. INTRODUCTION

Manufacturing processes of a graphene sheet can give rise to a wide range of intrinsic point and extended defects on its structural composition. Indeed, this material exposes an one-atom-thick surface and as a consequence their properties are deeply subjected to the interaction with the surrounding environment. This interaction is bound to induce various levels of disorder in these materials. Already from the growth stage and notwithstanding the possibility to obtain high crystalline quality at the micrometer scale, all popular growth techniques give rise to local or extended deviations from the ideal atomic structure (e.g. vacancies, Stone-Walles defects, chemi-absorbed adatoms etc.). A further source of structural disarrangement can be identified within patterning manipulations. Finally, the steps of device integration for these structures enhance perturbations and interactions with both dielectrics and contacts, giving rise to important alterations in their conductance characteristics [1].
The goal of this manuscript is to discuss the role of non-ideality on the electronic transport properties of graphene based system. We will show that a multi-scale approach, where *ab-initio* and *ab-initio* calibrated model are synergistically applied, is a reliable framework to reliably study the disorder effect in the conduction properties of these systems. A particular focus will be given to H damaged graphene, which can emerge after the detachment of the buffer layer due to H exposure in epitaxial graphene grown on SiC substrates [2].

2. METHOD

As reference system we consider pure and defected hydrogen-terminated armchair graphene nanoribbons AGNRs of different width and length ideally contacted (same width as the conductor without defect or impurity inclusion) at the right side and left size. The terminology of Ref. [3] is applied to categorize them on the basis of the dimer lines N along the ribbon width. Structural relaxation and atomic reconstruction are performed by means of the SIESTA *ab-initio* suite [4]. We use the Green function technique and the standard Landauer-Buttiker approach for the calculation of quantum transport [5]. Hamiltonians and overlap matrices are written directly within the first-principles approach or within semi-empirical models calibrated by means of first-principle calculations [6].

3. AB-INITIO RESULTS

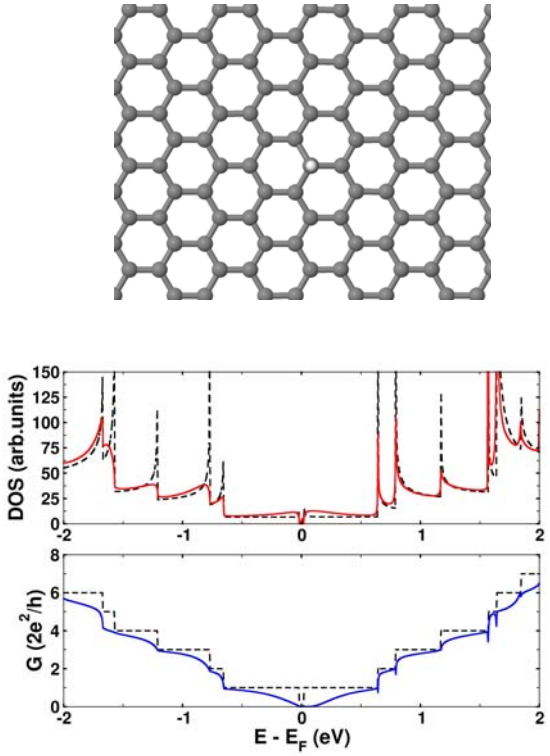

Fig. 1: (Upper panel) Top view of the stable configuration of an H adatom bonded to a graphene sheet in an on top configuration. (Central Panel). DOS of a pristine 20 AGNR (dashed black lines) and a H defected GNR (red solid line). (Lower Panel). Conductance in $G_0=2e^2/h$ of a pristine 20 AGNR (dashed black lines) and a H defected 20 AGNR (red solid line).

In fig. 1 we show a comparison between the Density of the States (DOS) and the low bias conductance as a

function of the energy in the cases of pure and H defected 20 AGNRs. The electron structure calculations have been performed on the optimized configuration (fig. 1 upper panel) where the H adatom resides in a on-top configuration and the bonded C atom looses its sp^2 character reaching a sp^3 configuration. DOS of defected system shows asymmetric alterations more pronounced in the valence band, whilst an increase of the DOS can be observed near the Dirac point $E-E_F=0$. In correspondence of this increased DOS a decrease of the conductance can is calculated due to resonant backscattering which is slightly displaced towards the conduction band. Note that, as we could expect, the H alteration of the conductance is similar to that of a "ideal" vacancy (infinite U center) in a bipartite lattice (see Ref. [6] for a discussion on this topic).

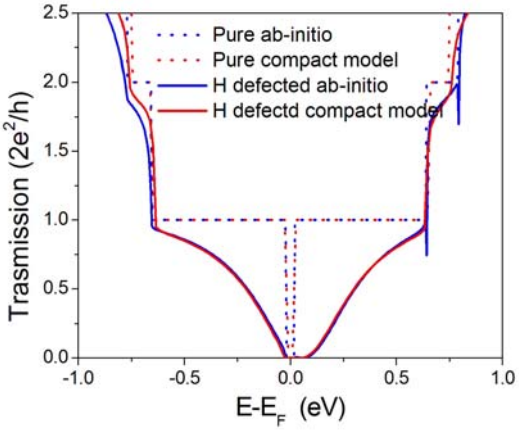

Fig. 2: Transmission as a function of energy calculated by means of ab-initio (blue) and ab-initio calibrated (red) models for pure (dashed lines) and H defected (solid lines) 20 AGNR.

4. CONDUCTION IN DISORDER GNRS

Calibrated semi-empirical models in the tight-binding scheme [6] can reproduce reliably the results of ab-initio electronic structure calculations using Hamiltonian with reduced complexity, which in turn allows to extend the analysis in large systems till to the μm scale. In order to demonstrate this statement we compare in fig. 2 the low bias conduction calculated by means ab-initio and calibrated methods in the 20 AGNR system. The agreement between the g(E) calculated by first principle methods and calibrated model is excellent.

The behavior of the average conduction in a semiconductor 47 AGNRs with length of the order of 0.1 μm and different density of H adatoms is shown in fig. 3. The alterations of the conductance are more significant near the resonance energies. However fluctuating values of g are calculated in the whole spectrum and the hole-electron symmetry is, in general, broken. Since, as we can expect, g(E) significantly changes with the disorder realization even when we fix the system's size and the density of scattering centers, in order to correlate systematically the conductance features to the average disorder status, a statistical analysis is needed using a large number of equivalent replicas of the same system. Coherent electron transport in a 1D system is characterized by the localization phenomenon firstly stated by Anderson [7]. The multiple interference due to random distributed scattering centers leads to an exponential increase of the 1D conductor resistance with its length L

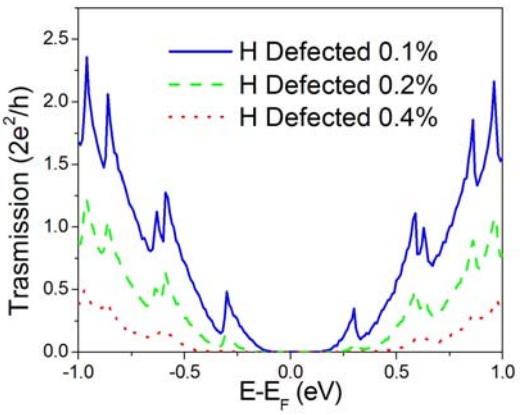

Fig. 3: Average conductance <g> as a function of the energy *E*, for H damaged N_a=47 AGNR with fixed length: L~0.10 μm and different adatom density. Statistical averages over more of 500 equivalent replicas of the system. Charge neutrality points of pure and defected systems are aligned at E=0 in the figure

We note that H defected GNRs are in the localization regime (for energy near the Dirac point) also for relatively low values of adatom density of the order of ~0.1 %. The mobility gap induced by the defects presence is substantially different from a real semiconductor gap since it is related to a huge density of state in the same energy range. Thus, the mobility gap cannot replace a real semiconductor gap for electronic applications. Finally we can observe the persistence of the conduction modulation with energy in disordered systems, related to the correspondent conductance plateaus of the subband structure in ideal GNRs.

5. CONCLUSION

We demonstrate, considering a particular case, that a multiscale approach based on ab-initio calculations is a reliable and efficient framework for simulating transport properties of graphene based device.

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STRAIN EFFECTS ON THE ELECTRONIC PROPERTIES OF GRAPHENE

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We study the dependence of the electronic band structure and of the optical conductivity of a graphene single layer on the modulus and direction of applied uniaxial strain. While the Dirac-cone approximation, albeit with a deformed cone, is robust for sufficiently small strain, band dispersion linearity breaks down along a given direction, corresponding to the development of anisotropic massive low-energy excitations. We recover a linear behavior of the low-energy density of states, as long as the cone approximation holds, while a band gap opens for sufficiently intense strain, for almost all, generic strain directions. This may be interpreted in terms of an electronic topological transition, corresponding to a change in topology of the Fermi line, and to the merging of two inequivalent Dirac points as a function of strain.

We propose that these features may be observed in the frequency dependence of the longitudinal-optical conductivity in the visible range, as a function of strain modulus and direction, as well as of field orientation. We also study the dependence of the plasmon dispersion relation of graphene on applied uniaxial strain. Besides electron correlation at the random-phase approximation level, we also include local field effects specific for the honeycomb lattice. As a consequence of the two-band character of the electronic band structure, we find two distinct plasmon branches. We recover the square-root behavior of the low-energy branch, and find a nonmonotonic dependence of the strain-induced modification of its stiffness, as a function of the wave-vector orientation with respect to applied strain.

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THEORETICAL INVESTIGATION OF THE STRUCTURAL, ELECTRONIC AND TRANSPORT PROPERTIES OF PURE AND INTERCALATED GRAPHENE ON SiC SUBSTRATES

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ABSTRACT

Epitaxial graphene on silicon carbide presents a combination of characteristics that render it highly attractive for device integration: wafer-size scales and direct growth on semi-insulating substrates. Here, based on extended first-principles and semiempirical calculations we discuss the structural, electronic and transport properties of graphene grown on both the silicon and the carbon face of SiC(0001) substrates. We show the fundamental differences of the Si and the C-face reconstructions and discuss their implications for the conduction characteristics of the two systems. We moreover explore the alterations expected with hydrogen or lithium intercalation and derive statistical expressions for the quantum transport properties of the resulting quasi-freestanding graphene.

1. EPITAXIAL GRAPHENE FROM *AB INITIO* SIMULATIONS

We start with a comparison of the surface reconstructions of the two faces of the SiC(0001) substrate. Results are based on extended *ab initio* calculations using commensurate supercells that minimize non-physical stresses. Si-face epitaxial graphene is characterized by the formation of a wide bandgap carbon-rich interface layer with a $6\sqrt{3}\times6\sqrt{3}R30^{o}$ surface reconstruction [Figure 1], over which Bernel stacked graphene layers of excellent quality grow [1]. However the interface interaction pins the Fermi level of the system above the charge neutrality point of neutral graphene, giving rise to a significant *n*-type doping for the entire system. Moreover the $6\sqrt{3}\times6\sqrt{3}R30^{o}$ reconstruction results in a significant substrate disorder below the buffer layer that can give rise to leakage currents through interface defects [2], compromising in a nontrivial way device-requested characteristics. On the other hand, growth on the C-face of SiC(0001) is less controllable with respect to the Si face but maintains a series of advantages regarding its electrical characteristics. The first carbon-rich layer here maintains a purely metallic character [3] and an important presence of π electrons, along with a non-negligible coupling with the substrate. The particularity of its geometrical configuration consists in a corrugated surface where small sp^2-bonded islands are terminated by carbon atoms that covalently bond with the substrate [Figure 2]. Below these islands also the surface carbon atoms sp^2-hybridize, while their π bands are half-filled and present a ferromagnetic order due to the presence of strong electron exchange interactions [3]. In this case there exists no Fermi-level pinning effect, allowing for a plausible device operation starting from an off-state. Typical graphene-like characteristics (i.e. the Dirac cone) are recovered with the addition of a second graphene layer [Figure 3].

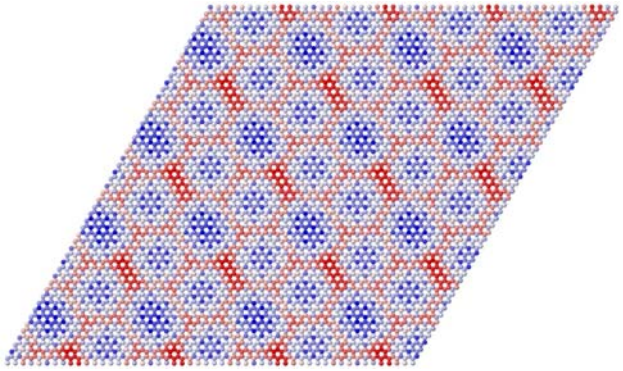

Fig. 1: Color map of the relative distance of the $6\sqrt{3}\times6\sqrt{3}R30^{o}$ buffer layer atoms from the SiC(0001) substrate, where gradual red to blue coloring indicates bigger to smaller distances. A (4 × 4) periodically reproduced unit cell is presented here.

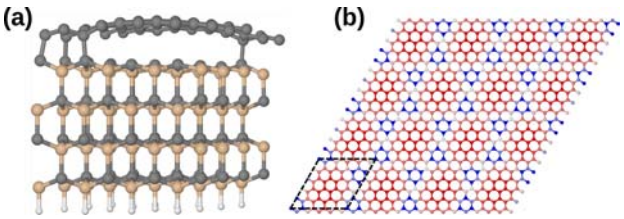

Fig. 2: (a) Side view of a (5 × 5) graphene monolayer relaxed on a (4 × 4) 4H-SiC($000\bar{1}$) substrate. (b) Color map view of the first epitaxial graphene layer showing the bonding characteristics of the carbon atoms, where gradual red to blue coloring indicates sp^2 to sp^3 bonding. Dashed lines show the periodically reproduced unit cell.

2. HYDROGEN AND LITHIUM INTERCALATION

As a remedy for the negative influence of the buffer layer in Si-face epitaxial graphene, intercalation with lightweight group 1 elements has been proposed [4][5]. Here, starting from the $6\sqrt{3}\times6\sqrt{3}R30^{o}$ reconstruction we study at an *ab initio* level structural and electronic properties considering hydrogen and lithium intercalation. In both cases the addition of the adatoms

successfully passivates the dangling bonds of the interface and restores order in the substrate. Structurally, the buffer layer is transformed in a flat graphene sheet. However the electronic properties of these two systems significantly differ, since only in the case of hydrogen intercalation the substrate maintains a semi-insulating character. When it comes to lithium, the metallic bands originating from the Li adatoms penetrate throughout the entire SiC bandgap, giving rise to an overall metallic behavior.

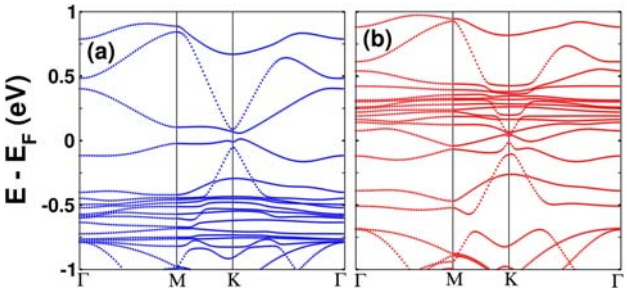

Fig. 3: Band structure of two graphene layers on a 4H-SiC(000$\bar{1}$) substrate for (a) the majority-spin and (b) the minority-spin configuration.

3. QUANTUM TRANSPORT

As a result of a non-ideal intercalation process, sp^3-type defects can be formed in the graphene epilayer due to a covalent bonding between the carbon and the hydrogen adatoms. Within a statistical study [6] of finite defect concentrations we explore the quantum transport properties of the resulting disordered quasi-freestanding graphene in terms of transport gaps [7] and fluctuations in the conductance distribution. Computations here are based on accurately parameterized semiempirical Hamiltonians from first-principles calculations and non-equilibrium Green's function techniques. We show that sp^3 hydrogen defects can give rise to extended transport pseudogaps around the Dirac point [see Figure 4] and significantly downscale the elastic mean free path of graphene even at relatively low concentrations. Finally, we discuss how our results can be interpreted for a consistent analysis of data deriving from experimental measurements.

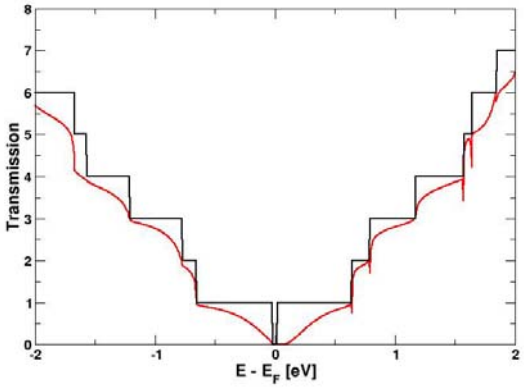

Fig. 4: First-principles description of the transmission probability as a function of energy for an armchair graphene nanoribbon with 20 dimer lines in the ideal configuration (black line) and in the case of a single hydrogen defect placed at the 10th dimer line (red line).

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SiC NANOWIRE FET OPERATION IMPROVEMENT BY USING SCHOTTKY CONTACTS AT SOURCE AND DRAIN REGIONS

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ABSTRACT

Back-gated field effect transistors (FETs) based on catalyst-free grown 3C-SiC nanowire (NW) were fabricated and the electrical characterization revealed electron conduction through the nanowires. Devices with either ohmic or rectifying contacts have been observed leading to two different operation modes. The transistors with ohmic-like contacts manifest very weak gating effect and the device switching off is not achievable even for high negative gate voltages due to the high electron concentration along the nanowires. In contrast, the Schottky contact barrier (SB) at Source (S)/ Drain (D) regions acts beneficially for the FET performance by suppressing the off-current. At high positive gate voltages (>20 V), the Schottky barriers tend to be more transparent leading to I_{ON}/I_{OFF} ratio equal to ~ 10^3 in contrast to the weak gating effect of the ohmic contact 3C-SiC NWFETs. Therefore, in the case of highly doped nanowires, SB-NWFET presents improved performance by suppressing the off current and indirectly modulating the drain current through the control of Schottky barriers transparency at source and drain regions.

1. INTRODUCTION

3C-SiC NWs combine the properties of 1-D material with that of SiC and electronic devices based on 3C-SiC NWs are expected to present concrete advantages in terms of dissipated power, stability and high voltage operation in comparison to their counterparts based on lower band-gap semiconductors.

The first experiments on 3C–SiC based NWFETs revealed that the carrier concentration is too high, due to unintentional doping, resulting in very low electron mobility. Possible causes for these high residual doping values are impurities contamination and/or large number of extended defects. It seems difficult to obtain monocrystalline SiC NWs without extended defects like SFs and low residual doping with the low cost 'chemistry-driven' methods used up to now [1]. Due to the high carrier concentration along the nanowire, SiC NWFETs with ohmic contacts present a very weak gating effect and could not be switched off even for very high negative gate voltage (-40 V) [2].

Hereby, it is proposed to use Schottky barrier (SB)-SiC NWFETs in order to suppress the off current and get an I_{ON}/I_{OFF} ratio equal to ~ 10^3.

2. EXPERIMENTAL

A simple catalyst-free process from low-cost reagents without subsequent purification step and allowing the preparation of large amounts of 3C-SiC NWs with tunable geometric features and surfaces, has been employed for the fabrication of the SiC NWs [3].

The process for the fabrication of the back gated SiC NWFETs included: (1) dispersion of the nanowires over a highly n-type doped Si substrate coated with 265 nm of SiO_2, (2) deposition of Ti/Au metallic pads around the nanowires, and (3) formation of metallic lines connecting (prior to this step, the NW native oxide was removed in buffered HF) the nanowire edges to the metallic pads by e-beam lithography and lift off process [4].

3. RESULTS AND DISCUSSION

The output characteristics of the rectifying (Schottky-like) behaviour contacts to the NWs before and after RTA are shown in Figs. 1a and 2a respectively. We observe that RTA converts a strongly asymmetric and non-linear I-V to an almost symmetric and much less sub-linear I-V with higher I_{on} current. This is quite probably due to the formation of Ni silicide during RTA process (NiSiC contact). In our case the thickness of Ni is 50 nm which is comparable with the nanowire diameter. This could result to a fully silicided nanowire at the contacts area permitting higher ON current. Due to the SB at S/D, the switching-off of the device is now possible both before (Fig. 1b) and after (Fig. 2b) RTA, resulting to an I_{ON}/I_{OFF} ~ 10^3. The linearly-scaled transfer characteristic (not shown) reveals a threshold voltage of about 4 V.

The weak gating effect of the ohmic-contact devices is a combined result of the high carrier concentration and the ohmicity of the contacts at source and drain regions that do not permit the modulation of the carrier concentration by the gate voltage. In the case of ohmic contacts (zero SBs), already for V_G=0 a significant current could pass through the nanowire by applying a small drain voltage,

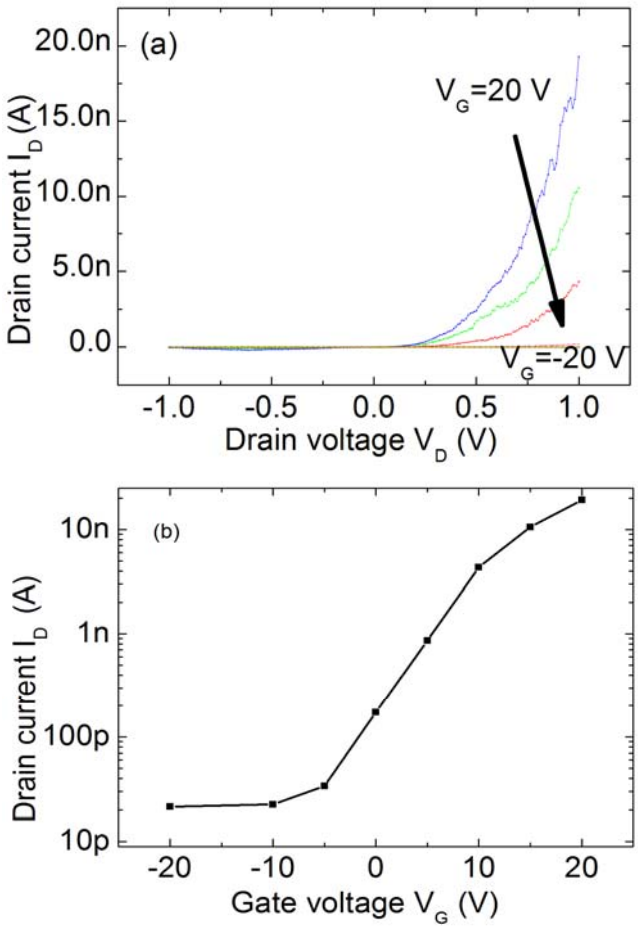

Fig. 1: (a) Output and (b) transfer characteristics of a SB-NWFET before RTA; transfer characteristics at V_D=1 V.

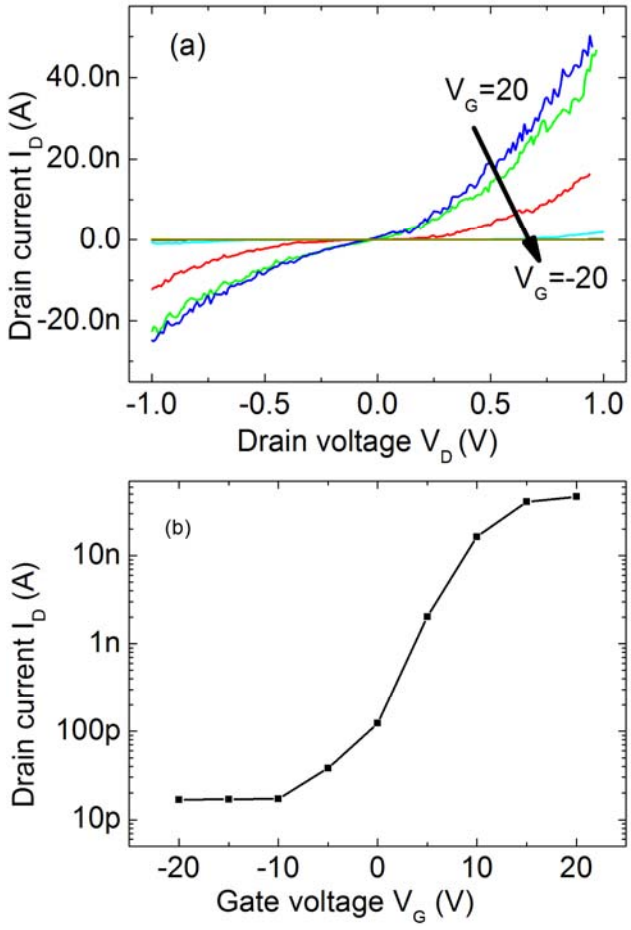

Fig. 2: (a) Output and (b) transfer characteristics of a SB-NWFET after RTA; transfer characteristics at V_D=1 V.

not allowing a V_G-dependent carrier modulation [2]. When a non-zero SB is present, the gate voltage could adjust the transparency of the barriers by appropriately moving the potential bands (back gate FET geometry), leading to a modulation of the drain current as it is shown in Fig. 10 of reference [5]. The maximum of the potential energy along the transport direction mediates the injection of the carriers from the source to drain through the channel potential barrier. The role of the external bias in a FET device is to appropriately modify the potential energy along the channel in order to maximize the current transparency independently the contact geometry. When a high gate voltage is applied (> 20 V) the effective Schottky barrier at the contacts is modified leading to increased tunneling current.

Note that effective Schottky barrier formation has been observed only for some devices of the same wafer due probably to a non-uniformity in annealing and/or NW doping level and/or high interface traps density as well as to the high sensitivity of the metal-NW contacts to local surface contaminations, which will result in a modification of the local effective value of the SB. The control and the origin of the SBs at source and drain regions of nanoFETs is still an open issue.

Therefore, given the high value of unintentional doping in SiC NWs, the use of SB contacts in source and drain is preferable. The SiC NWFETs with ohmic source and drain contacts perform poorly due to the fact that the doping in the nanowire is too high preventing the nanowire of becoming fully-depleted in the off-state. If nanowires with reduced doping could be grown then the ohmic contact devices would outperform the SB devices by a wide margin.

Another option for addressing the problem resulting from the high doping would be to use a smaller nanowire with a diameter enough small to be completely depleted. However, the depletion width at so high carrier concentration level is extremely narrow on the level of new nanometers (<5 nm) under zero external voltage. So it is not applicable in our devices and not suitable for the state-of-the-art technology of SiC NWs.

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1/10 LOW BIAS OPERATION AND INDIVIDUAL CHARGE DETECTION OF CARBON NANOTUBE QUANTUM NANO MEMORY

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ABSTRACT

10 times lower writing bias and individual charge transfer from nanotube channel to memory node was observed in the carbon nanotube (CNT) quantum nanomemory, in which the CNT with narrow diameter of ~1nm was used as a channel surrounded by the SiN/SiO_2 double layer insulators with the gold nano particle that works as a memory node.

1. INTRODUCTION

The problems of the present flash memory is its high applied gate bias of 20~25V to introduce the charges into the memory node. Using the ultra small diameter of carbon nanotube as a channel, the electric field concentration occur, and even at 10 timed lower applied gate bias of 2V, the enough electric field for the Fowler-Nordheim tunneling is obtained and charge can tunnel to reach the memory node. Using this phenomena, we have succeeded in fabricating the new memory.

2. STRUCUTRE OF CNT NANOMEMORY

Fig. 1 shows the schematic structure of the CNT quantum nanomemory. The distance between source and drain electrode is 2μm, and the gate length 100nm. The thickness of SiN_x and SiO_2 layers are 1nm and 10nm, respectively. The gold particles are placed at the interface of SiN_x /SiO_2 layers.

3. ELECTRIC FIELD CONCENTRATION

Because of the narrow CNT channel, the high-electric field concentration was generated even at the low applied gate bias, and charge in the nanotube is easily extracted by the Fowler-Nordheim tunneling through the insulater to the gold nano particle, and is trapped there. Fig. 2 shows the calculated (a) potential and (b) electric field distribution between the gate electrode and channel for the conventional planar type memory and the present CNT quantum nanomemory, when 3V top gate bias was applied. For the conventional planar type memory, the potential slope is mild and the electric field is as low as of the order of 10^6V/cm, and it is not enough value for the Fowler-Nordheim tunneling. For the CNT quantum nanomemory, on the other hand, the potential slope is sharp and the electric field is as high as of the order of 10^7V/cm, and it is enough value for the Fowler-Nordheim tunneling. Thus, even at low applied gate bias of ~3V, CNT quantum nanomemory shows the enough hysteresis though the conventional memory with planar type structure needs more than 20~25V for the writing bias. Thus, 10 times lower writing bias was realized using the CNT channel memory.

4. EXPERIMENTAL RESULTS: HYSTERESIS

Fig. 3 shows the experimental results of hysteresis characteristics of CNT quantum nanomemories (a) without and (b) with gold nano particle. In Fig.3(a), at the low applied top gate bias of 5V, the nanomemory shows the hysteresis. But at the applied top gate bias of 2V, the device shows almost no hysteresis. On the other hand, nanomemories with gold nano particle shows enough hysteresis even at the low applied bias of 2V. This is attributed the large trap site in the gold nanoparticle.

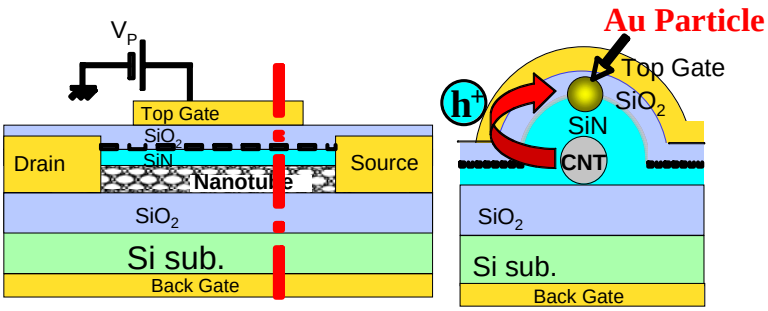
5. EXPERIMENTAL RESULTS: INDIVIDUAL CHARGE DETECTION

The threshold voltage of CNT quantum nanomemory showed the step like shift, i.e., at the applied gate bias lower than 300mV, the threshold voltage stayed constant value, and shifted suddenly around 260mV when the applied gate bias exceeds more than 300mV. This is attributed to the Coulomb blockade effect. The diameter of the gold nano particle that works as a memory node was measured by AFM and found to be ~2.5nm. The charging energy for the 2.5nm gold nano particle in the present device structure is calculated to be 300meV. Therefore, the step like shift of the threshold voltage is due to the single charge injection from the CNT channel to gold nano particle.

When the top gate bias comes back to 0V after the enough writing bias was applied, the step like jump of the drain current attributed by the single hole discharge was observed as shown in Fig 4.

6. CONCLUSIONS

In conclusions, we have succeeded in 10 times lower operation of nano memory and detected the one by one individual charge transfer.



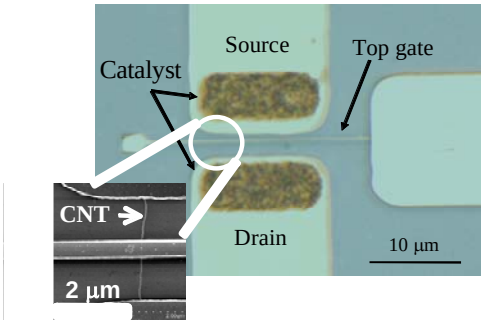
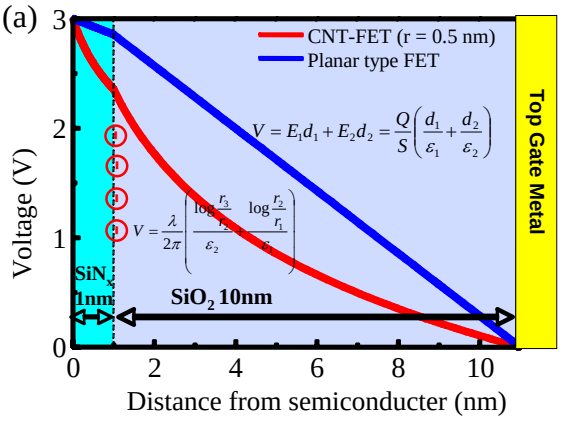


Fig. 1: Schematic structure & optical micrograph of quantum nano memory.



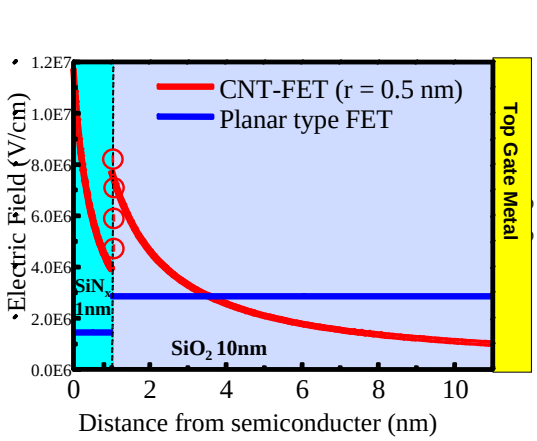
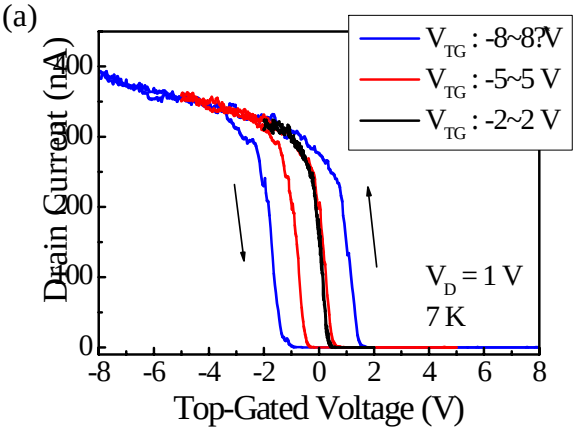


Fig. 2: Distribution of (a) potential and (b) electric field for conventional planar type memory and carbon nanotube memory.



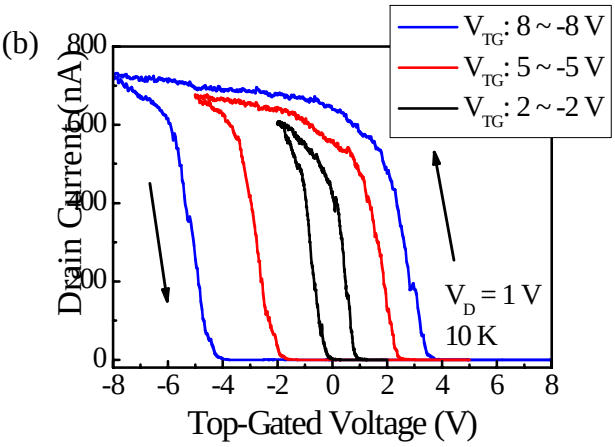


Fig. 3: Hysteresis of CNT-FET nanomemory (a)without and (b)with gold nano particle.

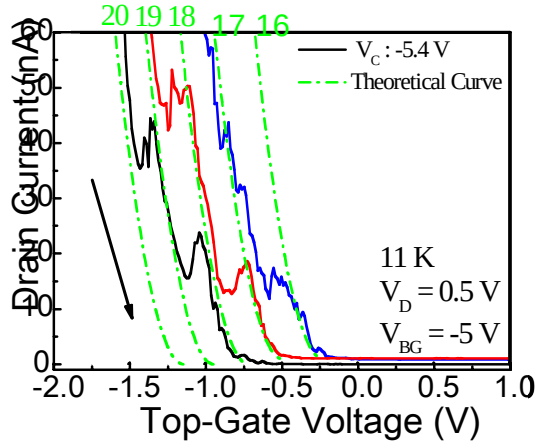


Fig. 4: One by one individual hole discharge from gold particle to nanotube.

FLEXIBLE CARBON NANOTUBE ARRAYS FOR PRESSURE SENSING WITH HIGH SPATIAL RESOLUTION

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ABSTRACT

Flexible vertically aligned multiwalled carbon nanotube arrays have been investigated under mechanical stress conditions. First experiments show the feasibility of highly sensitive piezoresistive sensors manifesting a resistance decrease up to ~35% and a spatial resolution of < 1 mm upon 10% compression. The results indicate that these CNT structures are well suited for pressure sensing.

1. INTRODUCTION

Carbon nanotubes (CNTs) have unique material characteristics with high electrical conductivity, supercompressibility, bending elasticity and structural flexibility. These make them an attractive material for pressure sensors. Freestanding films of vertically aligned carbon nanotubes have highly compressive behaviour up to 85%. The nanotubes can collectively form zigzag buckles that can fully elastically unload to their original length upon load release [1].
The integration of nano-dimensional carbon nanotubes into micro-components permitting the efficient use of their nano features, is one of the main challenges concerning their future technical implementation in higher organized device architectures [2]. This paper addresses aspects of this type by investigating CNT-based pressure sensor technology and their experimental characteristics including their special resolution.

2. FABRICATION

A porous 50 µm thick alumina with parallel, hexagonally arranged, cylindrical pores was used as nanostructured template. Vertically aligned, multiwalled nanotube arrays were produced by non-catalytic Chemical Vapor Deposition (CVD) in the alumina pores having an average pore diameter of 160 nm. The resulted CNTs had a length of 50 µm, a diameter of 160 nm and a density of 6×10^6 per mm^2 homogeneously distributed over the wafer. The highly aligned 3D CNT array structures use the carbon layer formed on the top and bottom of the alumina template for micro-nano integration, as well as mechanical stabilization.

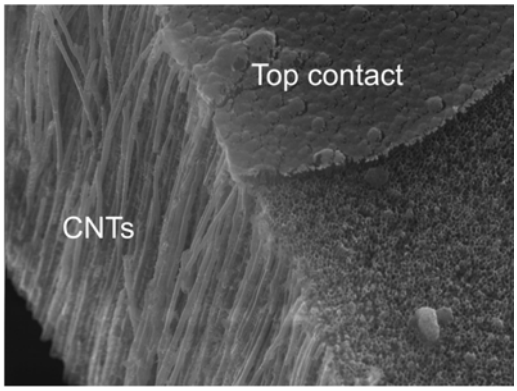

Fig. 1: SEM picture of the vertically aligned multiwalled carbon nanotube arrays with top contact. The resulted CNTs have a length of 50 µm and a diameter of 160 nm.

Several standard processing steps such as Au sputtering, optical lithography and etching were used for the CNT integration with microstructured patterns allowing easy access to the CNTs and monitoring of their characteristics. Finally, a wet chemical HF etching process was used to remove the Al_2O_3 template surrounding the contacted CNTs. This resulted in a negative carbon copy of the original template. Free-standing vertically aligned uniform CNTs could be obtained in this way (Fig. 1). The CNT arrays produced in this way are very promising candidates for pressure sensors, which are thin, flexible, stable, skin-like and 3D sensitive.

3. MEASUREMENT RESULTS

A home-built test platform was used to measure the displacement and compression of the CNTs in response to various loads. The loading stage consisted of a micropositioner with a needle and a piezoelectric stage providing the actuation. The needle at the micropositioner stage was pressed into the CNT array from the top contact which bottom side was glued on a ceramic substrate attached to a moving PZT stage. The changes of the I-V characteristics of the two-terminal pressure sensor under compression loading are shown in Fig. 2 for the case of 50 µm tall CNT arrays.

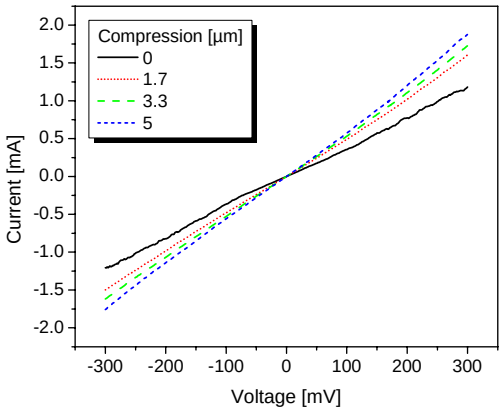

Fig. 2: I-V characteristics of the two-terminal pressure sensor under compression loading of 50 µm-long CNTs. The curves corresponds in different displacement lengths.

The sensing mechanism in the proposed configuration is due to a change of the number of CNTs contributing in the overall conducting current path. At certain compressive strain level, the mechanical deformation of the CNT arrays causes the change of CNT bundle conductance. The bent CNT bundle touches its neighboring free-standing CNTs and leads in a form of cross-tube coupling, which generates additional current paths and increases the conductance. Initial measurements of the integrated CNT bundle have shown a resistance decrease up to ~35% at compressive stress and local resolution smaller than 1 mm. Upon application of different compressive strain levels there are variable degrees in the change of conductivity, these recover well after strain removal.

The flexible CNT arrays were tested using a robotic test setup by Battenberg Robotic GmbH and measurement of the resistance variation was made over the sample. The study showed a spatial resolution of less than 1mm. This is not very different than the special resolution of finger tips, suggesting therefore the possibility of using the developed arrays as “artificial finger skin”.

4. SUMMARY

Micro-nanointegration of vertical CNT arrays was successfully demonstrated for pressure sensing. The 50 µm-long CNTs were highly linear and were terminated at the upper and bottom carbon layers perpendicular to the tube axis. A home-made piezoelectric set-up was used for sensitivity and spatial resolution investigations. First experiments show high sensitive piezoresistive sensors with a resistance decrease in the range of ~35%. The flexible sensor array can be mounted on a 3D surface and detects small deformations with a high resolution compatible with robotic requirements.

ACKNOWLEDGMENT

The assistance of Battenberg Robotic GmbH in evaluating the spatial resolution of the developed CNT arrays is greatly acknowledged.

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Session 4 :

Graphene devices

Chair : Prof. Phaedon Avouris

Monday May 30, 16:30 - 17:20

CHEMICAL VAPOR DEPOSITION OF GRAPHENE FOR BEYOND CMOS DEVICES

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ABSTRACT

Large area graphene films have been grown by chemical vapor deposition using a methane precursor on Cu substrates. The growth of graphene on Cu is unlike growth on other metal substrate in that growth takes place by a surface mediated process and not by a segregation-precipitation process as in the case of Ni, Co, Pt, Pd. The difference is a result of extremely low solubility of C in Cu even close to the melting point. Raman spectroscopy shows the presence of monolayers of graphite (graphene) over more than 95% of the Cu surface. Field effect transistors fabricated using CVD graphene on Cu also show that high mobility comparable to that found in exfoliated graphene can be achieved. However, significant more work needs to done in order to achieve the quality material with uniformity and quality required by the electronics industry.

1. INTRODUCTION

In the past decade, the state of the art Si-based electronics has gone from devices with a gate length of about 100 nm to 20 nm and below, with a defined pathway to devices, logic and memory, of about 15 nm. In addition, as devices have scaled below a gate length of about 100nm, performance per power density has not scaled.[1] In order to address the power issues the industry is facing as CMOS devices are scaled further, a new switch will have to be developed. Graphene, a mono-layer of carbon atoms arranged in a honeycomb lattice, has recently been the subject of considerable theoretical and experimental interest because of its unique transport properties together with exceptional chemical and physical properties. New devices taking advantage of the theoretical prediction on the existence of a Bose-Einstein Condensate in bi-layer-graphene films have been proposed[2,3], together with tunnel FETs[4] and a few others.[5] In order to demonstrate these new devices, high quality graphene films will be needed and will have to be integrated with dielectrics, metal electrodes and contacts. High quality graphene has been exfoliated from natural graphite. However even though these films have shown exceptional electrical properties they are usually only several tens of microns on the side. The successful demonstration and implementation of graphene-based device technology will require synthesis of much larger area graphene that can be grown directly on dielectrics on Si or can be transferred and integrated in a conventional Si device flow. The discovery of large-area graphene growth on Cu substrates has opened opportunities for the development of graphene-based devices on Si.[6] Growth of graphene on Cu by chemical vapor deposition (CVD) is unlike growth on other substrates such as Ni, Co, Pt or Pd, for example,[7] in that a self-limited monolayer of graphite is grown by a surface mediated process rather than a segregation-precipitation.[6] In order to take advantage of the fundamental properties of graphene it is necessary to grow uniform and nearly defect-free films as the semiconductor industry has done with silicon substrates. The growth of graphene on Cu and its properties will be reported in this short paper.

2. EXPERIMENTAL

Large area graphene films have been grown by CVD on Cu foils (99.8% purity)in a simple hot wall reactor using methane as the carbon source and hydrogen gas.[6] Figure 1 shows schematically the temperature-time and gas flow-time process used to grow graphene films on copper. The growth time of graphene can range from a few minutes to over one hour depending upon the specific growth conditions, temperature, methane pressure, and flow rate.

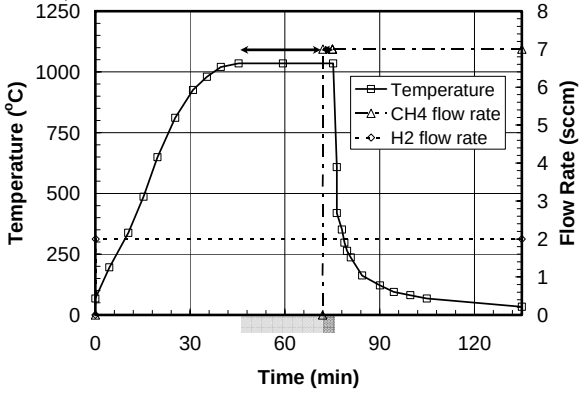

Fig. 1: Temperature and gas flow rate vs time plots during a typical graphene growth run on Cu substrates in a hot wall furnace.

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Graphene was was grown at temperatures around 1035 ºC, which is close to the Cu melting point. However, films can also be grown at much lower temperatures using methane or other precursors. The films were analyzed using Scanning Electron Microscopy (SEM), Raman spectroscopy and simple field effect transistors were fabricated and analyzed as previously reported.[8]

3. RESULTS AND DISCUSSION

Large area graphene films were grown in a hot wall reactor using methane gas with small amounts of hydrogen. What makes copper special for CVD growth of graphene is its low carbon solubility and mild catalytic activity. The equilibrium phase diagrams of Cu-C and Ni-C clearly show that the solubility of C is very small in Cu and high in Ni.[9] There are a few values of solid solubility reported in the literature and they vary by about one order of magnitude, from about $7x10^{17}$ cm^{-3} to $2x10^{19}$ cm^{-3} as determined by combustion with in-situ infrared spectroscopy.[10,11] Fig. 2 shows a secondary ion mass spectrometry concentration profile of C in Cu and Ni after annealing in methane at 1000ºC and ~1100ºC respectively followed by fast cooled to room temperature. The C concentration is clearly very uniform in the case of C in Cu up to the the surface of the foil. This concentration of C in Cu after cooling of about $1.3x10^{19}$ cm^{-3} is in the same range as the published solubility values. In the case of Ni there is clearly a concentration gradient as a result of C segregation and precipitation at the surface of the Ni with 100% carbon at the top of the Ni substrate. The "bulk" values of C shown in the SIMS profiles cannot be considered as solubility limits of C in Ni or Cu because the samples were not quenched fast enough to freeze in the high temperature C concentration.

Fig. 3 shows the Cu surface coverage as a function of time for 3 different methane partial pressures at a constant growth temperature of 1035ºC. The data indicates that by increasing the partial pressure of methane the Cu coverage rate increases. In the case of low pressure, however, full coverage is not achieved. Further, the growth rate decreases with time as the domains get closer. The decrease in growth rate as a function of coverage is due to a decrease in catalyzed carbon source because as a result of a decrease in available Cu. However by increasing the precursor flow rate the Cu surface can be fully covered with graphene. In the case of full coverage at short times the graphene domain size or equivalently the 2D grain size can be small, less than 5 μm, i.e. the nuclei density is high at higher pressures. In order to increase the domain size or 2D grain size a two-step process was developed by Li et al. where domains up to about 20 μm were reported.[12,13]

Very large domain size, single crystal, films have also been demonstrated by growing under lower gas flow rates and pressure, conditions promoting a low nuclei density.[13] The growth rate under these conditions is constant at about 1.2μm/min at the growing lobes, and the number of nuclei is much lower than films grown under the so called standard conditions. The constant growth rate with time is attributed to the constant availability of C_xH_y from the Cu surface in comparison to conditions of impinging domains.

As in the case of most semiconductor devices it is highly likely that graphene device performance will be influenced by point defects and line defects. If so, then it is critical that single crystal graphene layers be grown with as few defects as possible and no grain boundaries. The experiments by Li et al. [13] suggest that "large", about 0.5mm, single crystals can be grown at near stagnant flow conditions as established by electron diffraction analysis and LEEM.

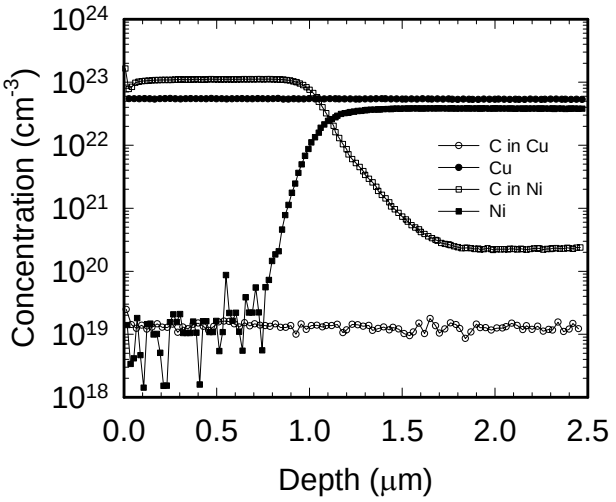

Fig. 2: SIMS profile of C in Ni and Cu after fast cooling from high temperature (1000ºC for Cu and ~ 1100ºC for Ni).

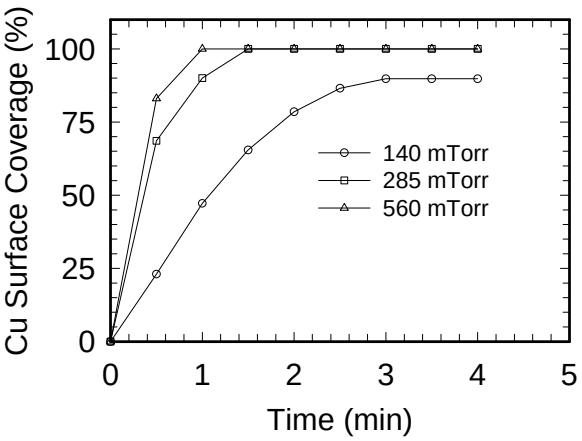

Fig. 3: Copper surface coverage by graphene as a function of time at 1035 ºC for various methane partial pressures.

Figure 4 shows an SEM image of a graphene single crystal grown on Cu similar to the process used by Li et al..[13] In comparison, the image of exfoliated graphene at the same magnification is shown in the top left hand corner of the image showing how much larger the CVD graphene single crystal can be. However nucleation and growth of a graphene single crystal over a large area, e.g. on a 300 mm diameter Si wafer, is still a challenge at this time but not necessarily unrealizable. After all, just a few

years ago we did not know how to grow graphene films at all over large areas and today polycrystalline graphene growth over arbitrarily large areas using Cu substrates is routine.[6,14] The quality of graphene grown on Cu has been studied by both Raman spectroscopy as well as transport measurements using back gated field effect transistors.[6]

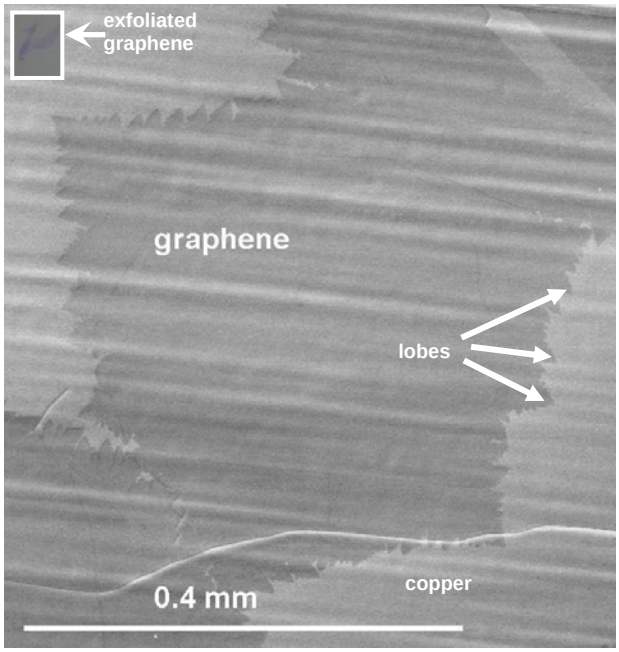

Fig. 4: Large area single crystal graphene grown in a copper pocket in nearly stagnant flow conditions as reported by Li et al. [13]. The insert is an optical micrograph of a typical exfoliated graphene flake for comparison purposes of the same magnification.

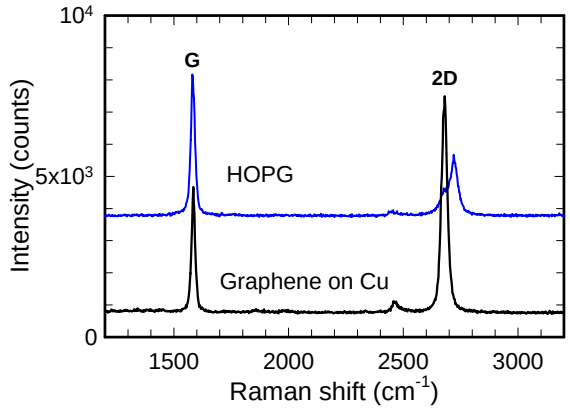

Fig. 5: Raman spectrum of graphene grown on Cu by CVD in comparison to highly oriented pyrolithic graphite (HOPG).

The Raman spectrum has several features that have been correlated to the quality of the graphene film.[15] For example the presence and intensity of the D-band, found around 1350 cm^{-1}, has been associated with point defects and some edge defects. Figure 5 shows the Raman spectrum of graphene grown on Cu in comparison to that of HOPG. The Raman D-band intensity in graphene is very low, within the noise level however there can be regions, like wrinkles and defects at domain boundaries within the polycrystalline graphene that can give rise to a larger D-band. The carrier mobility of graphene grown on Cu has been studied and reported elsewhere and will not be reviewed here but suffice it to say that it is comparable to that of exfoliated graphene and improving as growth and transfer processes are improved.[12]

4. SUMMARY AND CONCLUSIONS

Graphene single crystal films are required to provide high quality devices for beyond CMOS scaling. Chemical vapor deposition has been demonstrated to have great potential for the growth of large single crystal graphene films. Assuming that graphene can show the needed device performance for beyond CMOS devices, high quality single crystal graphene will be needed to meet the stringent uniformity requirements typical for the electronics industry. We are still in the initial stages of graphene materials and device development and much work will be needed before graphene can be implemented in a real device flow.

ACKNOWLEDGMENTS

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PERFORMANCE PREDICTIONS FOR GRAPHENE-WINDOW SCHOTTKY-BARRIER SOLAR CELLS

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ABSTRACT

Photovoltaic conversion efficiencies for graphene/semiconductor Schottky-barrier solar cells are estimated using a comprehensive analytical model. Present and possible values are considered for important graphene properties: optical transmittance, sheet resistance, and work function. Promising results are predicted for CdTe thin-film absorbers, but not for Si single-crystal substrates.

1. INTRODUCTION

In the quest for a low-cost, practical photovoltaic device, Schottky-barrier solar cells employing graphene are beginning to be investigated [1,2]. The main motivation for this type of diode is the elimination of the need to form a *p*-*n* junction. The main attractions of graphene for the metallic layer are: high optical transmittance over much of the solar spectrum [3]; low sheet resistance [4]; an ability to tune the work function by chemical doping [2,5], or by interfacial-layer modification using synthesized polymers [6], or by the formation of multiple layers [7]. Values for the work function of graphene appear to range from 4.3 eV (single layer [7]) to about 4.9 eV (multiple layer, interface-modified [6]). For the semiconducting absorber, *p*-type doping is likely to be preferable as, in most common semiconductors, electrons (the minority carriers) have the higher diffusivity and diffusion length. Thus, in order to obtain a low dark current, a semiconductor with a high bandgap and a graphene layer of low work function are desirable. Here we concentrate mainly on CdTe, for which the bandgap is 1.5 eV. Some results are also presented for Si, as graphene/*n*-Si Schottky-barrier solar cells have already been reported [1]. However, the relatively low bandgap of this material is unlikely to lead to Schottky-barrier solar cells of comparable efficiencies to *np*-junction cells [8].

2. THE MODEL

The equations for photocurrent generation in the depletion region and the quasi-neutral base of a solar cell are well known [9, pp.123-124], and are used in this work. A base doping density of 1E16 cm^{-3} is considered, along with a front-surface recombination velocity of 100 cm/s and an ohmic back contact. For thin-film p-CdTe, the electron diffusivity and diffusion length are taken to be 8.3E-4 m^2/s and 6.4E-7 m, respectively [10]. The corresponding values are taken to be 27.4E-4 m^2/s and 1.64E-4 m for high-quality *p*-Si [9, Fig. 7.7], and 11.5E-4 m^2/s and 2E-5 m for holes in *n*-Si [9, Secs. 3.2.4, 5.4.1]. For both CdTe and Si the electron affinity is 4.05 eV. Semiconductor thicknesses were taken to be 3 microns for thin-film CdTe and 450 microns for single-crystal Si.

The standard equation for the dark current in a Schottky diode was used [9, p.198], along with values for the barrier height (in eV) of 1.25 for *p*-CdTe, 0.87 for *p*-Si, and 0.86 for *n*-Si. These numbers were obtained using values for the graphene work function of 4.3 eV in the *p*-semiconductor case, and 4.9 eV in the *n*-semiconductor case, *i.e.*, the reported values that would result in the most favourable (highest) barrier heights.

For the absorption coefficient data, values for CdTe were taken from Ref. [11], and from Ref. [12] for Si. AM1.5G illumination was used, and the cell temperature was assumed to be 300 K.

The graphene series resistance was estimated for a square cell of side 1 cm, with resistance-less contacts along two opposite sides. Values for the sheet resistance RS of graphene were taken to be (in ohms/square): 400, 100, 10, 4. These values correspond, respectively, to: the best obtained to-date for films with an optical transmittance TO of 90% at 550 nm; the minimum industry standard for TO=90%; the best likely value for doped graphene at TO=90%; the best likely value for doped graphene at TO=80% [13].

In the results that follow, TO was taken to be either 80% or 90% across the entire AM1.5G spectrum.

3. RESULTS AND DISCUSSION

The J-V curves under AM1.5G illumination for the *p*-CdTe solar cells are shown in Figure 1. For a perfectly transmitting and conducting graphene film the photovoltaic conversion efficiency is 16.8%. This drops to 16.3% when TO is limited to 90% and the sheet resistance is the lowest that is likely to be attained (10 ohms/square). At the same TO, but with RS at the industry-minimum value of 100 ohms/square, *i.e.*, the value needed to be competitive with indium tin oxide films, the efficiency drops further to 11.6%. The worsening fill-factor is the reason for these changes. The change is dramatic when graphene of the lowest sheet resistance attained to-date (400 ohms/square) is used. In this case the short-circuit current is also affected, and the

efficiency drops to 4.0%. If TO=90% is not attainable, and a more realistic value proves to be 80%, then Fig. 1 indicates that a high fill-factor is possible if RS can be reduced to 4 ohms/square. The efficiency in this case is 14.7%.

For comparison purposes, at TO=90% and RS=10 ohms/square, the best conversion efficiencies for cells on *p*-Si and *n*-Si are 8.1 and 5.3%, respectively. The higher barrier height in the *p*-type case leads to a larger open-circuit voltage V_{oc}, and the superior minority carrier properties lead to a higher photocurrent. The Si values are much lower than the corresponding value of 16.3% for CdTe, primarily because of the latter's much higher V_{oc}, which is a direct result of the higher barrier height, which, in turn, is due to the higher bandgap.

4. CONCLUSIONS

From this simulation study of Schottky-barrier solar cells employing a graphene window layer it can be concluded that:

- photovoltaic conversion efficiencies with thin-film, *p*-type CdTe can match those of conventional CdS/CdTe cells, providing single-layer graphene of work function 4.3 eV , optical transmittance 90% and sheet resistance 10 ohms/square can be attained;
- the range of achievable work functions for graphene does not allow sufficiently high barrier heights to be obtained with either *p*- or *n*-type Si for competitive Schottky-barrier cells to be expected from this semiconductor.

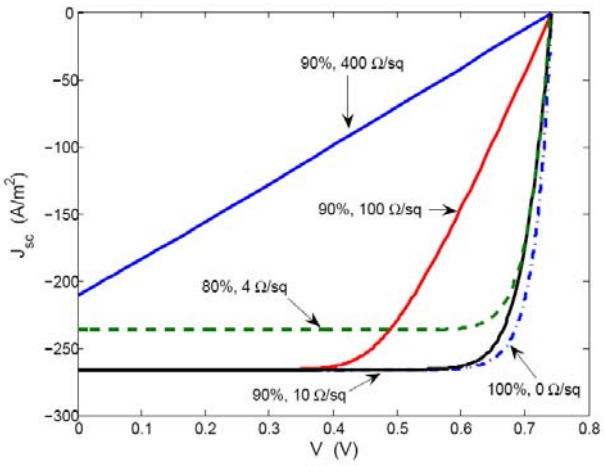

Fig. 1: J-V curves under AM1.5G illumination for a graphene/*p*-CdTe solar cell with graphene of the optical transmittance and sheet resistance indicated.

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COVALENT FUNCTIONALIZATION OF GRAPHENE TOWARDS A BIOLOGICAL TRANSDUCER

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ABSTRACT

Exfoliated graphene has been shown to easily sp^3 functionalize through a low temperature radical addition comparable to known processes in carbon nanotubes (CNT)[1]. Similar chemistry will be applied to graphene grown on semi-insulating SiC via high temperature sublimation. Graphene will be covalently functionalized through a low temperature addition process involving 4-nitrobenzene diazonium tetrafluoroborate. The modified graphene surface will provide the perfect template for further chemical functionalization into specific molecular binding sites. The binding site functionalized graphene on SiC will then be processed into resistors and field effect transistors (FETs) for DC and AC electrical measurements. Solution-based binding of bio molecules will be investigated for changes in graphene's electronic properties. Sensitivity, accuracy, and speed will be compared to that of current enzyme-linked immunosorbent assay (ELISA) technology.

1. INTRODUCTION

Graphene is a material under immense recent investigation. Measured electron mobilities has exceeded 100,000 cm^2/Vs[2]and physical robustness even in atmospheric conditions above 250° C makes graphene a unique material for electronic devices. However, graphene's chemical proximity to organic molecules and large atomic binding energy also makes it a promising material for quick response electronic biological transducers without fluorescence.

Large area graphene on copper foil as wide as 30" has been successfully transferred via roll to roll technique[3]. These properties along with graphene's zero bandgap and low bending modulus allows for the possibility of a low power micro-bio transducer in a light-weight flexible format.

2. GROWTH

Graphene will be grown by high temperature sublimation of Si from SiC substrates. Samples will be grown via a two filament heating systems with growth temperatures ranging from 1350° C to 1600° C and pressures ranging from 10^{-6} torr to atmospheric conditions. Monolayer graphene on si-face step-bunched surface will be grown. These samples will be tested against the rougher multilayer graphene grown carbon face surfaces for sensitivity and binding speed.

3. FUNCTIONALIZATION

Graphene will be initially functionalized with nitro-benzene groups via both an electrochemical and thermal process. This reaction involves the radical addition of 4-Nitrobenzendiazonium in water and other solvents.

After initial functionalization, the Nitros group will then be further functionalized with bio-sensitive chemical species. Specific binding sites for polar molecules will be attached first in order to produce the largest electronic response in graphene.

4. MATERIALS CHARACTERIZATION

4.1. Atomic Force Microscopy (AFM)

AFM will be used to characterize sample surfaces through each stage of chemical modification. Scans from the same location will be compared to see physical topographical differences induced by sp^3 hybridization and further bio-functionalization.

4.2. Raman Microscopy

The relative intensity of the D peak will be compared pre and post functionalization to determine the degree of sp^3 hybridization.

4.3. Fluorescence Spectroscopy

This technique will be used to determine functionalization of the nitro-benzene group and the bio-specific binding sites.

4.4. Potentiometry

Potentiostat measurements will be used to determine the speed of binding onto functionalized graphene surfaces. Initial experiments seem to suggest extremely fast reaction times especially in very thin graphene samples.

5. DEVICE PROCESSING

Resistive and Impedance measurements will be performed on graphene electrodes of various sizes ranging from 5um to 20um. Top gated Field Effect transistors will be made in various sizes ranging from 5-40 um.

6. DEVICE TESTING

All device testing will be performed with the assistance of Robert Congdon from Sadik's group at Binghamton University. Sensititivity, accuracy and speed will be compared to current commercial technology.

7. SUMMARY

Graphene grown on SiC will be functionalized with attachment of 4-nitrobenzene group. These samples will be further functionalized with bio-sensitive binding sites. Electrical testing of electrodes and FETs will be performed. Results will be compared to commercially available products.

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GRAPHENE FETs WITH SiCN GATE STACK DEPOSITED BY PECVD USING HMDS VAPOR

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ABSTRACT

SiCN thin film is used as a gate stack for graphene channel FETs. The SiCN is deposited by plasma-enhanced chemical vapor deposition (PECVD) using hexamethyldisilazane (HMDS) vapor with hydrogen carrier gas. This approach has an advantage in the cleaning effect in graphene surface by means of hydrogen. Symmetric ambipolar behavior with the conduction minimum at zero gate voltage is observed in the output characteristics of the fabricated FETs.

1. INTRODUCTION

Graphene is becoming one of important candidates of high-mobility channel materials for field effect transistors because of its large room-temperature mobility [1]. Indeed a cutoff frequency of over 100 GHz has been reported for graphene FETs with a gate length of 240 nm [2]. A gate stack is also a key to achieve good FET characteristics. In addition, the gate stack/graphene interface should be controlled. Hence the pre-cleaning of graphene is also important in the gate process, for which hydrogen annealing is reported to be efficient [3].

This paper reports the plasma enhanced chemical vapor deposition (PECVD) of SiCN that is applied to the gate stack of graphene FETs. The hydrogen-based gas used in this PECVD becomes an advantage on graphene FETs from the viewpoint of the surface cleaning. Resulting FETs exhibit good ambipolar characteristics.

2. DEVICE FABRICATION

Graphene was prepared by the thermal decomposition of SiC substrates [4,5]. A semi-insulating 6H-SiC substrate is used as a starting material. The sample was annealed at 1700°C for 15min in ultrahigh vacuum to form graphene on its surface. The cross sectional view of a graphene FET is shown in Fig. 1. The device fabrication started by the ohmic metallization (Ti/Pd/Au) with e-beam evaporation. Then the channel isolation was carried out by oxygen plasma etching. As the gate stack, SiCN thin film was deposited by PECVD using hexamethyldisilazane (HMDS) vapor [6]. The PECVD system is shown in Fig. 2. The storage tank of liquid HMDS is heated at 60°C and the temperature of the gas line was kept at 100°C to introduce HMDS vapor into the reactor. The gate process was carried out as follows: First the sample was annealed in hydrogen ambient to clean the graphene surface. Next HMDS vapor was introduced in the reactor in addition to hydrogen. The mixture ratio of HMDS and hydrogen was 1:25. After the pressure was stabilized at 133 Pa, PECVD was carried out at 350°C. A 10-nm-thick SiCN was deposited on graphene. The dielectric constant was estimated to be 4. After PECVD, the gate metal (Ti/Pt/Au) was evaporated and lifted off.

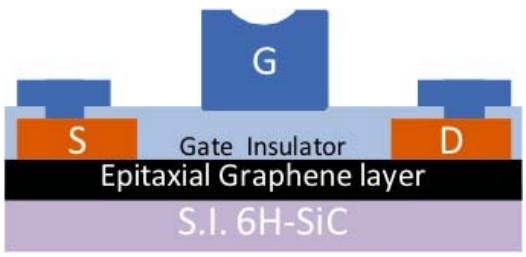

Fig. 1: Cross section of graphene FETs.

3. RESULTS AND DISCUSSION

We fabricated graphene FETs with a gate length of 3 μm. Figure 3 shows the drain current (I_d) as a function of the gate voltage (V_{gs}) at a drain voltage (V_{ds}) of 1.5 V. The fabricated FETs exhibit good ambipolar characteristics with the conduction minimum at zero gate voltage. The transmission line model (TLM) measurement reveals the contact resistance of 0.38 Ω.mm. The transconductance was 35 mS/mm for n-type operation and 33 mS/mm for p-type operation at a drain voltage of 1.5 V. The field effect mobility was estimated to be 300 and 280 cm^2/V.s for electrons and holes, respectively. This result suggests that SiCN deposited by

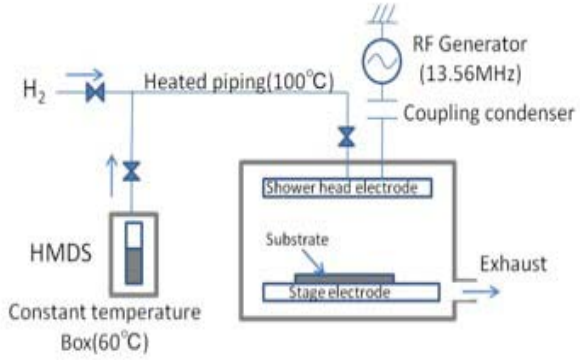

Fig. 2: Diagram of PECVD system.

PECVD using HMDS vapor and hydrogen forms good

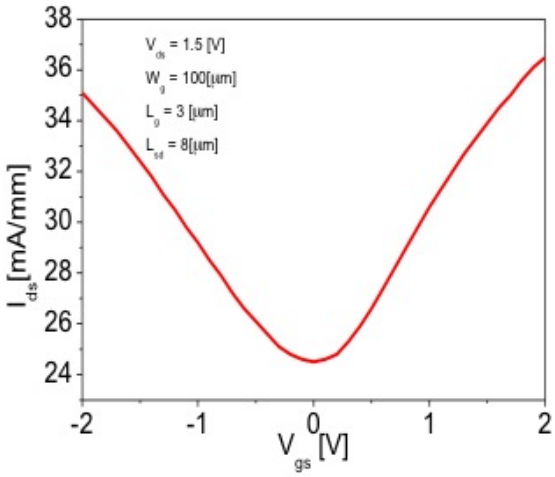

Fig. 3: Drain current versus gate voltage of 3-μm-gate graphene FETs (Drain voltage: 1.5 V).

interface with the graphene channel due to the cleaning effect by hydrogen. Therefore it is also applicable to an interfacial layer of high-k gate stack such as Al_2O_3.

4. CONCLUSION

Graphene channel FETs were successfully fabricated by using SiCN gate stack deposited by PECVD using HMDS vapor with hydrogen carrier gas. The device exhibits symmetric ambipolar characteristics in the output characteristics.

ACKNOWLEDGEMENTS

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Session 5 :

Thermal effects, reliability and packaging issues

Chair : Prof. Gaudenzio Meneghesso

Monday May 30, 17:20 - 19:00

EFFECTS OF SUBSTRATE AND BUFFER LAYER QUALITY ON THE BEHAVIOR OF AlGaN/GaN HEMTs : THERMAL EFFECTS VERSUS ELECTRON TRAPPING

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ABSTRACT

In this work, AlGaN/GaN HEMTs have been grown on various substrates like silicon, 4H silicon carbide, 3C-SiC on silicon, GaN or AlN on sapphire templates and free standing GaN. Material studies show good quality materials with threading dislocation density and electron mobility depending on the choice of the substrate. Transistors with 3-4 µm micron gate length have been fabricated. DC and pulsed current-voltage measurements show that the main limitations are related to thermal dissipation. In some cases a more complicated situation appears with additional electrical traps.

1. INTRODUCTION

The development at a large scale of high frequency/high power III-nitride field effect transistors is known to be a hard task due to the lack of large diameter lattice matched substrates. For these reasons, alternative substrates such as silicon, 3C-SiC on silicon or (GaN, AlN) templates on sapphire are proposed for reducing the cost, each of them presenting its own advantages and drawbacks. In order to clarify the effect of substrate choice on layer quality and transistor behavior, AlGaN/GaN HEMT heterostructures have been grown on such substrates as well as on 4H-SiC and on free standing (FS) GaN obtained by thickening and separation of an initial GaN on sapphire seed.

2. MATERIAL GROWTH AND STUDIES

The structures have been grown by molecular beam epitaxy using NH_3 as a nitrogen source [1,2]. Specific developments have been necessary to overcome the residual doping present at the regrown interface on GaN templates or substrates [3]. The crystal quality is routinely assessed by X-ray diffraction and atomic force microscopy in order to estimate the amount of threading dislocations (TDs). Plan-view transmission electron microscopy confirms the observed trends [4]. As shown in Table 1, for heterostructures with similar active layers (AlGaN barriers with an Al molar fraction of ~ 29 % and 1 nm thick AlN spacer) a correlation is observed between the density of TDs and the electron mobility within the 2-dimensional electron gas (2DEG) at the barrier/channel interface, the mobility attaining 2000 cm²/V.s at 300K once a TD density below $4x10^9$/cm² is reached. Furthermore, lowering the temperature exacerbates the difference in carrier mobility as shown by the comparison of HEMTs grown on Si(111) with ones on MOCVD GaN template. One noticeable point for transistor applications is the relatively low background doping level in the GaN buffer layers recorded by C-V measurements after pinch-off of the 2DEG.

Substrate	Si(111)	3C-SiC	Sapphire	Sapphire	FS GaN
			MOCVD-GaN	MOCVD-AlN	HVPE
GaN buffer thickness	0.5-1.7 µm	1.7 µm	4-7 µm	2 µm	300 µm
Dislocation density (/cm²)	3-10x10^9	<5x10^9	<1x10^9	2-3x10^9	1x10^7
2DEG density (/cm²)	0.8-1x10^{13}	1.1x10^{13}	1x10^{13}	9x10^{12}	9.7x10^{12}
RT electron mobility (cm²/V.s)	1650-2100	2050	2030-2150	2085	2180
max LT electron mobility (cm²/V.s)	13700		31000		
Residual doping level n (cm^{-3})	2-4x10^{14}	1-2x10^{14}	<3x10^{14}	<3x10^{14}	1x10^{14}

Table 1: Crystal quality and electrical properties of AlGaN/AlN/GaN HEMTs grown on different substrates

3. DEVICE RESULTS

In order to evaluate the interest of these structures, transistors with typically 3-4 µm micron gate length have been fabricated. The device process involves mesa definition by $Cl_2/Ar/CH_4$ based reactive ion etching, TiAlNiAu ohmic contact and NiAu Schottky contact deposition. The devices are not passivated. Transistors with 9-12 µm source-drain spacings exhibit a maximum drain current density in the range of 400-600 mA/mm and transconductances in the range of 100-120 mS/mm. The drain leakage current at pinch-off is low and at 100 µA/mm and 50 µA/mm at Vds=20 V on GaN and AlN templates on sapphire respectively; it is as low as 65 µA/mm on FS GaN, whereas it is in the range of 60-100 µA/mm on silicon and 20 µA/mm on 4H-SiC. DC output characteristics of the transistors show a drain current collapse which is in a first view dependent with the thermal conductivity of the substrate, the lower collapses being observed on 4H-SiC and FS GaN, the higher on (GaN, AlN) templates on sapphire and intermediate ones on silicon. The drain current collapse plotted in Fig.1 is calculated using the drain current Id_{knee} in the knee region (Vds<6V) and the current Id_{20V} recorded at Vds=20V:

$$collapse = (Id_{knee} - Id_{20V}) / (Id_{knee})$$

At low current levels, only a drain current saturation occurs so that this parameter appears as negative.

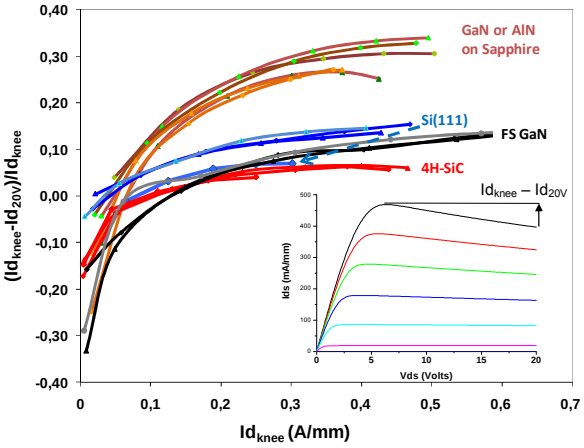

Fig. 1: Drain current collapse measured in DC conditions.

Pulsed current-voltage measurements (600 ns, 100 Hz) performed on devices on sapphire and on silicon substrates confirm the primary importance of thermal effects (Fig.2). However, it appears that the devices on silicon with the thicker GaN buffer layers and then with a resulting reduced TD density show an increase in both the DC and pulsed drain current collapses. To explain these behaviors, the competition between additional thermal barriers in the buffer layers and electron trapping by dislocations has to be taken into account. These measurements show that structures on silicon with thinner buffer layers benefit from more efficient heat dissipation and surprisingly a higher dislocation density may induce more electrically stable devices.

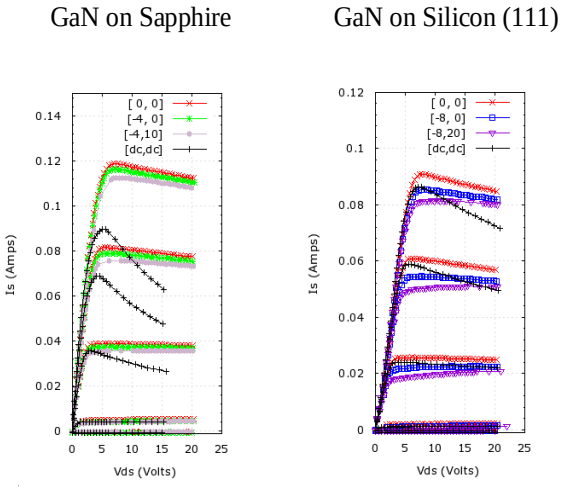

Fig. 2: DC and pulsed measurements performed on HEMTs on silicon and sapphire substrate.

4. CONCLUSION

In this work, we have studied AlGaN/GaN HEMTs grown by molecular beam epitaxy on various substrates. We have shown that the material quality and the electron transport properties are mainly dictated by the lattice parameter mismatch between GaN and the chosen substrate or template. We have observed that the DC drain current collapse is mainly driven by the thermal conductivity of the substrate. Pulsed measurements performed on sapphire and silicon confirm this point. However, it appears that the devices on silicon with the thicker GaN buffer layers and then with a resulting reduced TD density show an increase in both the DC and pulsed drain current collapses. On the opposite structures on silicon with thinner buffer layers benefit from more efficient heat dissipation and surprisingly a higher dislocation density may induce more electrically stable devices.

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THE IMPACT OF BARRIER SURFACE TREATMENT ON AlGaN/GaN HEMT RELIABILITY

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ABSTRACT

Reliability of AlGaN/GaN HEMTs processed with different surface cleaning steps was studied using electrical and optical methods. It was found that HEMTs with surface treatment leading to surface oxides formation are more susceptible to degradation in terms of gate leakage and trapping characteristics, although these oxides seem to passivate surface traps. This indicates that oxygen related trap states may play a crucial role for AlGaN/GaN HEMT reliability.

1. INTRODUCTION

Although AlGaN/GaN HEMTs are able to handle unprecedented RF power, their reliability and long-term stability are still major concerns [1]. In particular, there is rather little known about the role of device fabrication on subsequent device reliability. It has been shown that different types of surface cleaning prior to nitride passivation and gate formation have a strong impact on the gate breakdown voltage [2]. In this work, the reliability of production-quality AlGaN/GaN HEMTs with two different surface treatments was studied using a novel electrical-optical methodology developed in [3].

2. EXPERIMENTAL DETAILS

GaN-capped AlGaN/GaN HEMTs grown by MOCVD on SiC substrate were fabricated using standard III–V processing technology. Prior to passivation layer deposition, the samples received different cleaning treatments using chemicals with different levels of oxygen content referred to as cleaning A and B in the following. X-ray photoelectron spectroscopy and Auger electron spectroscopy analysis showed a surface oxygen content of about 20% and 30% for samples with cleaning A and B, respectively, indicating a more pronounced surface oxidation of the GaN cap layer for the latter. Devices with 400 μm gate width were stressed in off-state condition at V_{ds}=30 V, V_{gs}=-5 V and base plate temperatures (T_b) 25, 100, 150, and 200 °C. Electrical characteristics in DC and pulsed mode together with trapping characteristics similar to [3] were measured. Electroluminescence (EL) imaging was employed to gain insight into the changes in lateral electric field distribution upon stressing.

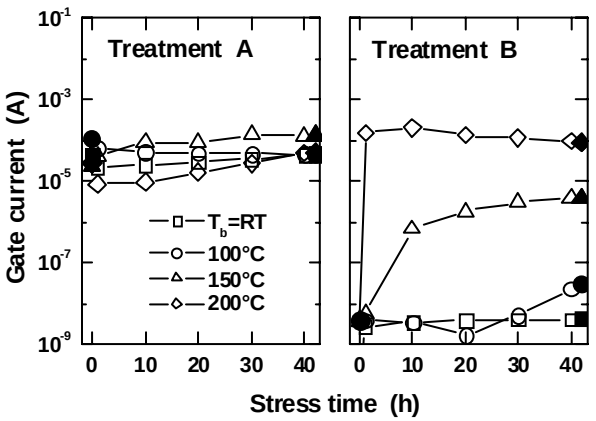

Fig. 1: Gate leakage current (V_{gs}=-7 V and V_{ds}=10 V) measured before and one day after (solid symbols) and during (open symbols) off-state stress as a function of T_b.

3. RESULTS AND DISCUSSION

Although HEMTs after cleaning B show four orders of magnitude lower gate current (I_g) than for after A (Fig. 1) and small gate-lag (Fig. 2) in a fresh state, both parameters progressively degrade for B and eventually approach about the same values as measured on HEMTs with cleaning A after off-state stress performed at T_b higher than 150 °C. In contrast, devices A show relatively high I_g and gate-lag, however, both parameters remain stable upon off-state stress for all T_b-s.

To compare the stress induced trap generation in HEMTs with different surface treatments, drain current (I_d) trapping analysis reported in [3] was employed. Fig. 3 compares I_d trapping analyses of HEMTs with cleaning A and B before and after stress performed at T_b=200 °C. Peaks reveal the trap time constants and relative trap densities. There are three traps apparent in the devices denoted as Tp1, Tp2, Tp3, where we focus mainly on Tp1 in the following. The time constant of Tp1 was found to be temperature dependent with an activation energy of ~0.5 eV, hence similar to trap Tp1 reported in [3,4] that was proposed to be related to oxygen defect complexes. In contrast to devices A, for HEMTs with cleaning B off-state stress increased the number of all traps significantly (Fig. 3). Detailed evolution of the Tp1 amplitude upon device stressing at different T_b-s is shown in Fig. 4.

From the gate-lag and I_d trapping analysis data, it can be concluded that HEMTs with higher surface oxide

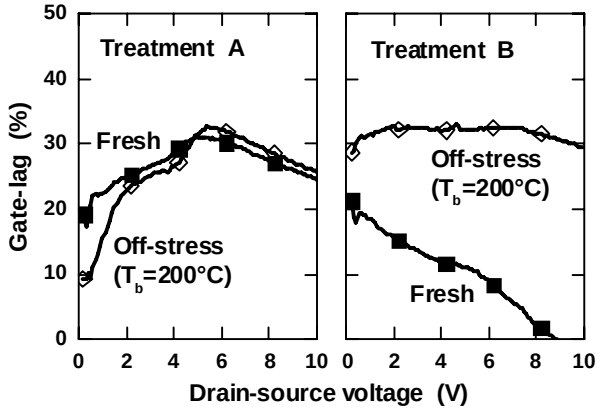

Fig. 2: Gate-lag as a function of V_{ds} measured before and after off-state stress performed at T_b=100 and 200 °C on HEMTs with different surface treatment. Pulsed characteristics were measured with 100-ns-long gate voltage pulses.

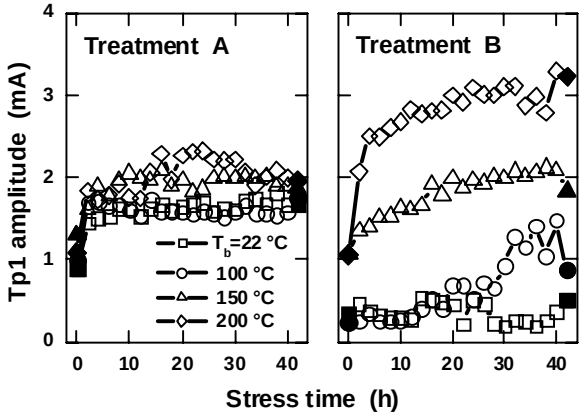

Fig. 4: Evolution of Tp1 amplitude before and one day after (solid symbols) and during off-state stress (open symbols) performed at different base-plate temperatures.

content show much faster trap generation upon off-state stress, consistent with their I_g evolution, although these devices showed lower initial trap densities compared to devices with lower surface oxide content. To confirm the importance of trap generation, the associated electric field distribution was probed using EL. The comparison between EL distributions before and after stress (T_b=200 °C) measured on HEMTs with treatment B shows an apparent decrease of EL intensity in the access region close to the drain side of the gate, as shown in Fig. 5. This is consistent with trap generation on the drain side of the gate edge, also observed in our previous studies [3]. In contrast, no significant change in EL was observed for devices after cleaning A.

Our results suggest that oxides on top of the GaN cap layer may passivate surface traps (Figs. 2 and 3). However, this oxide may not be stable enough and disintegrates when exposed to high electric fields and elevated temperatures. As trap generation is temperature activated (Fig. 4), oxide disintegration could be driven e.g. by oxygen diffusion or drift from the surface region into the top device and/or SiN layer as proposed in [4] for T_b above 150 °C. This assumption would be consistent with the higher Tp1 amplitude for devices B compare to A stressed at T_b=200 °C, corresponding to oxygen incorporation into the barrier subsurface region as an

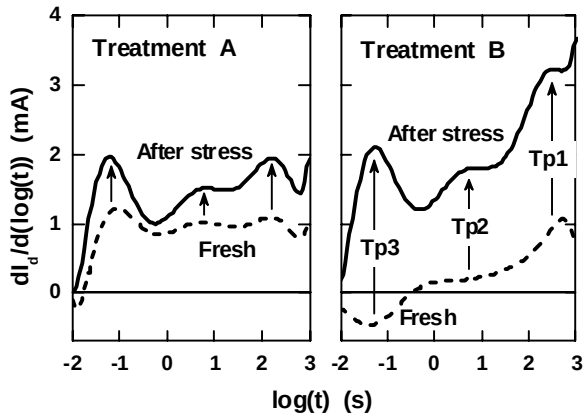

Fig. 3: Derivative of I_d transients in logarithmic scale before and after off-state stress performed at T_b=200 °C revealing dominant traps denoted as Tp1, Tp2, and Tp3.

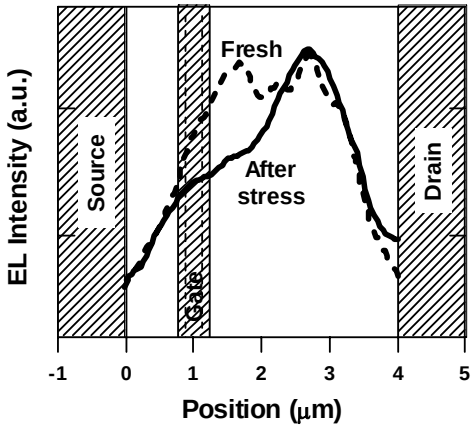

Fig. 5: Electroluminescence (EL) distribution before and after off-state stress (T_b=200 °C) on HEMT after cleaning B.

electrically active complex, however, other impurities may also play a role.

4. CONCLUSIONS

It was found that HEMTs processed with cleaning steps leading to surface oxides formation are more susceptible to degradation in terms of gate leakage and trapping characteristics, although these oxides seem to passivate surface traps in the device prior to stressing. This indicates that oxygen related trap states may play a crucial role for AlGaN/GaN HEMT reliability.

ACKNOWLEDGEMENT

CDTR (University of Bristol) is grateful for support from the ONR and ONR Global (N00014-08-1-1091) through the DRIFT program (monitored by Dr. Paul Maki).

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THERMAL CHALLENGES OF WAFER BONDING OF AlGaN/GaN HEMTS

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ABSTRACT

By wafer bonding, N-polar GaN HEMTs as well as the transfer of AlGaN/GaN HEMTs to high conductivity substrates can be realized from standard HEMT structures. This work demonstrates the impact of the bonding layer thickness on the thermal properties of AlGaN/GaN HEMTs on the example of N-polar GaN devices, which are analyzed by Raman thermography in combination with thermal simulations. Bonding layers less than 100-200 nm are found to be essential for achieving acceptable device thermal characteristics.

1. INTRODUCTION

AlGaN/GaN HEMTs offer great opportunities for high power and high frequency applications. Despite their excellent performance, device reliability and thermal management are still major concerns for this technology. Wafer bonding has recently been explored by various industrial and research laboratories, motivated by the potential for improving the thermal and electrical properties of GaN-based HEMTs, such as achieving N-polar GaN HEMTs [1] as well as transferring epilayers to high thermal conductivity substrates, e.g. diamond [2].

In this work, the impact of wafer bonding transition layers on the thermal properties of AlGaN/GaN HEMTs is studied on the example of N-polar GaN-based devices fabricated by transfer and wafer bonding onto silicon substrates. The device temperature was assessed by micro-Raman thermography and further analyzed by thermal simulations focusing on the impact of the bonding layer thickness on the thermal properties of the devices investigated.

2. EXPERIMENTAL AND SIMULATION DETAILS

Ga-face AlGaN/GaN devices grown on Si substrates by MOCVD were bonded onto a Si(100) wafer for the fabrication of N-polar GaN devices. Direct wafer bonding technology via a 700-nm-thick PECVD-grown SiO_2 layer was used. Further details on the fabrication of the devices can be found in Ref. [1]. For comparison, a Ga-polar GaN device grown directly on a Si substrate was also studied. The device temperature was assessed by micro-Raman thermography, which uses a laser source to probe lattice vibrations in the active region of the device with sub-micron spatial resolution [3]. Ungated AlGaN/GaN structures with a contact spacing of 25 µm and a width of 100 µm were operated at 12 W/mm, to assess the thermal characteristics of the device layer structure. Raman measurements were performed at the centre of the device. Three dimensional thermal simulations were also performed considering a thermal conductivity for GaN and Si of 160 $m^{-1}K^{-1}W$ ($\sim T^{-1.4}$) and 130 $m^{-1}K^{-1}W$ ($\sim T^{-1.3}$), respectively. The interlayer between the GaN and the Si substrate for as-grown devices or the bonding layer after wafer bonding was treated in the model as thermal boundary resistance (TBR) similar to Ref. [4].

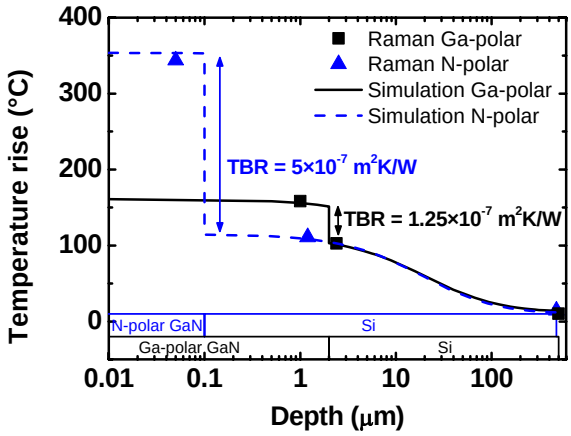

Fig. 1: Temperature depth profile measured by Raman thermography on ungated AlGaN/GaN devices, overlaid with a thermal model for Ga-polar and N-polar device structures. The inset schematic shows the layer structure of the two samples. Interface layers were treated as thermal boundary resistance (TBR) in the model.

3. RESULTS AND DISCUSSIONS

The temperature depth profile of a standard Ga-polar AlGaN/GaN ungated device on a Si substrate is shown in Fig. 1. The temperature step between the measured GaN and Si temperature reflects the presence of a TBR related to the AlGaN-based transition layer between the GaN layer and the Si substrate. This interlayer hinders heat transport from the GaN into the Si substrate. We note that this TBR is somewhat higher than TBR measured

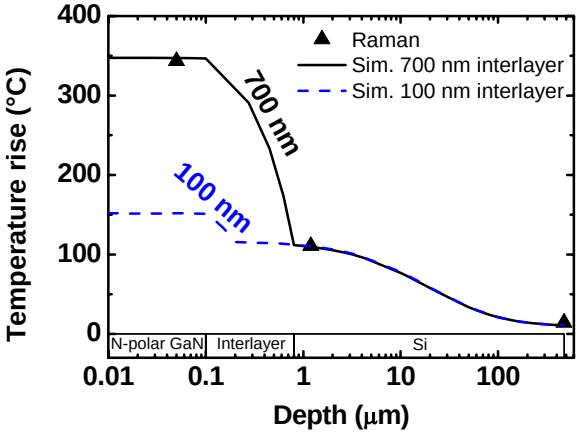

Fig. 2: Temperature depth profile of an ungated N-polar AlGaN/GaN device with a 700-nm-thick interlayer between the GaN and the Si substrate, from Raman measurements. Also shown is a thermal model with parameters fitted to the Raman results.

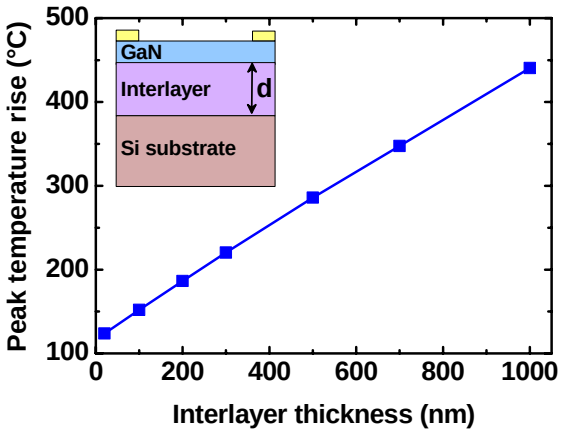

Fig. 3: Predicted peak temperature rise in ungated N-polar AlGaN/GaN devices estimated from thermal simulation for different interlayer thicknesses between GaN and Si substrate.

previously for GaN-on-SiC [5], and it reflects the low thermal conductivity of the AlGaN transition layer. After using a 700 nm bonding layer to achieve N-polar devices, the TBR increased to 5×10^{-7} $W^{-1}m^2K$ resulting in a significantly higher peak channel temperature compared to the standard Ga-polar device, as shown in Fig. 2. Device temperature increased by a factor of 3-4, i.e., there is a significant temperature increase across the 700-nm-thick bonding layer. To be able to fit the device temperatures measured by micro-Raman thermography, an interlayer thermal conductivity of $1.18\ m^{-1}K^{-1}W$ ($\sim T^{0.3}$) was needed to be introduced in the model to correspond to the measured TBR. This illustrates that a low thermal conductivity of the bonding layer can provide challenges, which can only be alleviated by reducing the thickness of the bonding layer or by considering alternative higher thermal conductivity bonding layers. As an example, Fig. 2 shows the effect of a 100-nm-thin interlayer, illustrating that a significant reduction in thermal resistance can be achieved with respect to the 700-nm-thick bonding layer.

Fig. 3 illustrates the predicted peak channel temperature rise as function of interlayer thickness. A large increase of the device temperature with increasing interlayer thickness emphasises the important role the bonding layer properties play for thermal management in AlGaN/GaN HEMTs. This demonstrates that the optimization of bonding layer thermal properties and its thickness is essential for achieving acceptable device reliability and lifetime. For the case considered here, less than 100-200 nm thickness of the bonding layer is desirable for achieving good thermal device properties.

4. CONCLUSIONS

The thermal properties of Ga-polar and wafer-bonded N-polar AlGaN/GaN devices were studied by micro-Raman thermography and thermal simulations. The results illustrate the importance of considering interlayer thermal properties and thickness for device thermal management. This is also of relevance to new technologies such as AlGaN/GaN HEMTs on diamond substrates, which require optimized bonding techniques to fulfill their potential advantages.

ACKNOWLEDGEMENTS

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TWO-DIMENSIONAL TRANSIENT SIMULATIONS INCLUDING TRAPPING AND THERMAL EFFECTS IN GaN HEMTs

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ABSTRACT

AlGaN/GaN high electron mobility transistors (HEMTs) have great potential, thanks to the unique material properties of III-N compound. However, there are still some problems with AlGaN/GaN HEMTs, such as thermal dissipation and parasitic effects induced by trapping phenomena that severely limit the power performances of these transistors.
The aim of this work is to gain insights into the degradation by means of 2-D numerical simulations.
In particular, transient tests are useful both to study the self-heating effect and to characterize such trapping behavior.

1. INTRODUCTION

For GaN based devices, the device temperature and deep level effects can vary with each DC bias, causing unacceptable errors between RF performance and model predictions. Deep levels are sometimes referred to as traps, and traps can be associated with either surface states or defects and impurities in the bulk semiconductor. The latter cause dispersion in the I-V characteristics.
The effects of self-heating related thermal effects on drain/gate lag have been ignored in the simulations, and few numerical works [1] have been reported on the drain lag simulation taking buffer trapping into consideration for GaN-based devices. This paper presents an approach for analyzing GaN devices that takes both thermal and trapping effects into account.
In particular, pulsed I-V tests are useful for any device where self-heating can be expected to affect the I-V performance, like AlGaN/GaN HEMTs. So, we consider such kinds of tests, which are based on the use of a pulsed source to stimulate a transistor or device under test (DUT), followed by a pulse measurement on the device.

2. DEVICE AND PHYSICAL MODELS

The $Al_{0.25}Ga_{0.75}N$/GaN HEMT analyzed to illustrate our results has a width of 200 μm and is reported in Fig.1. The two-dimensional device simulator used in this work was ATLAS by Silvaco Inc. [2]. Poisson's equation and continuity equations for electrons and holes are solved, and a drift-diffusion model is used to solve transport equations. Electron saturation velocity and mobility model are taken according to Farahmand's theory [3]. As the gate is a Schottky contact, a barrier $\phi_{Schottky}$ of 1.0 eV

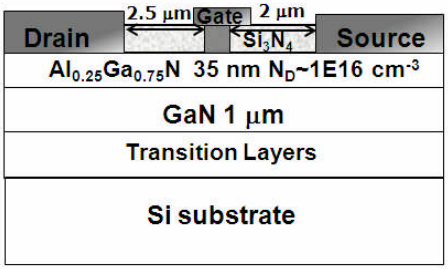

Fig. 1: Schematic cross section of the HEMT analyzed.

is considered. The built-in fields due to spontaneous polarization and strain (piezoelectric effect) are taken into account as fixed sheet charges: a positive sheet charge $+\sigma_{POL}$ with density 0.8×10^{13} cm^{-2} was defined at the AlGaN/GaN interface, and the equivalent negative sheet charge $-\sigma_{POL}$ was defined at the AlGaN surface. Surface states are included through a fixed donor trap density σ_T, uniformly distributed on the un-gated source-gate and gate-drain regions. Simulation results, shown in the next paragraph, have been obtained with surface traps energy level equal to 0.95 eV, related to the valence band, and density $N_{DT}=5\times10^{12}$ cm^{-2}.
Additional sources of charge, such as bulk GaN, have been included. All the acceptor bulk traps have concentrations of 0.5×10^{16} cm^{-3} with energy levels of 0.5 and 0.3 eV below the conduction band. The dynamic traps are modeled by a Shockley–Read–Hall recombination term, included in the continuity equations. An additional differential rate equation is solved to account for emission and capture processes in transient trap simulations. Electron and hole capture cross sections of 1×10^{-15} cm^2 are used for all trap levels, which are consistent with other reported 2D numerical simulations [4]-[5]. The module GIGA extends ATLAS for lattice heat flow and for the dependence of material and transport parameters on the lattice temperature [2]. The heat flow equation is added to the primary equations that are solved by ATLAS. For AlN and GaN, a temperature dependent thermal conductivity is considered: $\kappa=K_{300}/(T/300)^{\alpha}$. For GaN, K_{300} is set equal to 1.6 W/cm K and $\alpha=0.28$, while for AlN, $K_{300}=2.85$ W/cm K and $\alpha=1.64$.

3. NUMERICAL RESULTS

In Fig. 2, pulsed Ids–Vds characteristics were measured using a pulse width of 1 μs. Gate and drain quiescent points (Vgs0, Vds0) are (Vp, 0 V) and (Vp, 25 V) for a) and b) respectively, where Vp is the pinch-off voltage.

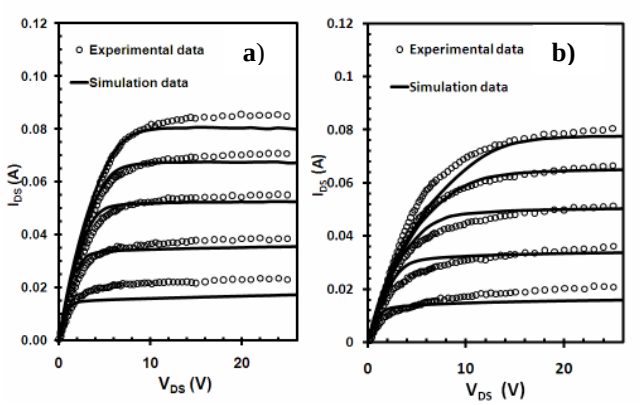

Fig. 2: Experimental Ids-Vds characteristics (white circle) and simulation data (solid line).The gate is pulsed from -4 V up to 0 V with a 1 V step.

This bias condition allows the drain-lag effect due to bulk traps to be individuated. Such types of measurements were useful to calibrate the trapping parameters and also the mobility model used. Furthermore, when the quiescent drain voltage is equal to zero, the ionized buffer traps effect is negligible and the gate-lag phenomena become visible (Fig.3). It is possible to notice that there is not a strong decrease of the drain current. As a consequence, the passivation with Si_3N_4 is a good mean to limit the gate-lag effects [6].

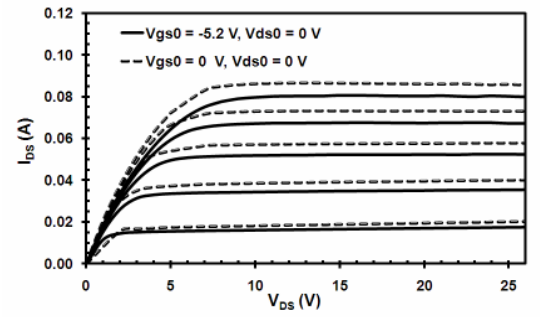

Fig. 3: Simulated Ids-Vds characteristics. The gate is pulsed from -4 V up to 0 V. The quiescent points for gate and drain are: (-5.2 V, 0 V) solid line; (0 V, 0 V) dashed line.

Figure 4 shows the transient response using the gate-lag and the drain-lag turn-on technique. For the gate-lag, a fixed voltage is applied to the drain terminal (10 V), and the gate is pulsed from the pinch-off (-5.2 V) to open channel condition (0 V).While for the drain-lag technique, a transient voltage is applied to the drain terminal (Vds=10 V), maintaining a fixed gate bias of Vgs=0 V. Two different behaviors are underlined: thermal and trapping phenomena. The initial drop in drain current (up to $3x10^{-5}$ sec. in Fig. 4.a) is caused by local self-heating in the channel. Indeed, the decrease in drain current that stretches over many decades disappears when the device temperature reaches a steady-state condition (see Fig. 4.b). As this effect vanishes, the traps play a key role. The drain current starts to increment at ~10^{-3} s, as shown in the inset in Fig. 4.a. When traps start to emit the trapped electrons, there is an increase in the 2DEG concentration in the GaN channel. As a consequence, the device drain current starts to rise [5]. Besides, the gate-lag and the drain-lag turn-on technique show all the traps'

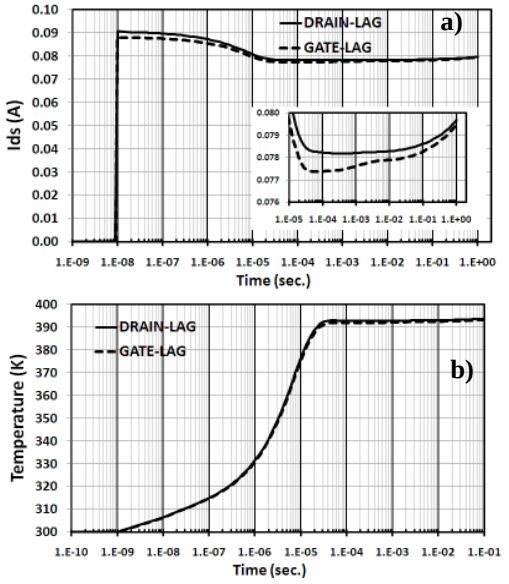

Fig. 4: **a)** Simulated Ids(t) transient response obtained using the gate-lag (dashed line) and the drain-lag (solid line) turn-on technique at Vds=10 and Vgs= 0 V, respectively. **b)** Device temperature during the transient simulations.

contributions with different time constants, due to the different energy levels considered (see the inset Fig.4.a).

4. CONCLUSIONS

In this work, the intrinsic mechanisms of drain/gate lag in AlGaN/GaN HEMTs are studied by using transient simulations. Starting with the positive agreement with experimental data, we can affirm that TCAD simulations are an invaluable instrument for predictive analysis at the design stage. As some trapping effects are very difficult to reduce or eliminate, the characterization of the relevant trap states is crucial for the optimization of GaN-based transistor performance.

ACKNOLEDGEMENT

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REVERSE CURRENT THERMAL ACTIVATION OF AlGaN/GaN HEMTS

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ABSTRACT

The objective of this paper is to analyze the impact of the high temperature (*T*) on on-state and, in particular, the reverse leakage currents (gate, drain and bulk) of AlGaN/GaN HEMTs in the temperature range of 25-310 ºC. Up to 150 ºC, the leakage current exhibits a weakly increase with *T* (E_a ~ 0.02 eV). At higher temperatures, the activation energy is much higher with E_a ~ 0.20 eV and 0.40 eV for drain and gate leakage currents, respectively.

1. INTRODUCTION

AlGaN/GaN high electron mobility transistor (HEMT) has emerged as one of the preferred power switch with great potential for many applications at high frequency, high voltage, and high temperature. To provide reliable transistors for these demanding applications it is necessary to evaluate the device performance at elevated temperatures. The objective of this paper is to analyze the impact of the high temperature (*T*) on the reverse leakage currents (gate, drain and bulk) of AlGaN/GaN HEMTs in the temperature range of 25-310 ºC.

2. EXPERIMENTAL DETAILS

AlGaN/GaN HEMTs were fabricated on a previously optimized stack to obtain a crack-free GaN layer (up to 2–3 µm) on commercial Si(111) [1]. This nucleation and buffer layer was basically formed by 250 nm of GaN and 250 nm of AlN. Then, a 1.7 µm GaN layer was molecular beam epitaxy (MBE) grown at 800 ºC, followed by the active layers. The active layer of the HEMT consists in a 1 nm AlN spacer to reduce alloy scattering and to enhance the electron mobility, and a 21 nm undoped AlGaN barrier with 0.28 Al mole fraction. Finally, the structure was covered with an additional 5 nm GaN cap layer. The device isolation was achieved by means of a 150 nm deep mesa etch realized by Cl_2/Ar reactive ion etching (RIE). Source/Drain Ohmic contacts were formed by a Ti/Al/Ni/Au annealed for 30 s at 750 ºC by rapid thermal annealing. HEMT gate contact was made with a Ni/Au bi-layer.

3. RESULTS AND DISCUSSION

It has been reported [2] that the drain leakage current is due to the injection of the electrons into the GaN buffer layer and the tunneling leakage current of the Schottky-gate reverse bias. In this sense, we have investigated the gate-source, the drain-source and the drain-bulk reverse currents in order to evaluate potential activation mechanism due to the temperature. Fig. 1 shows typical I_{ds}-I_{gs} and transconductance vs *T* curves.

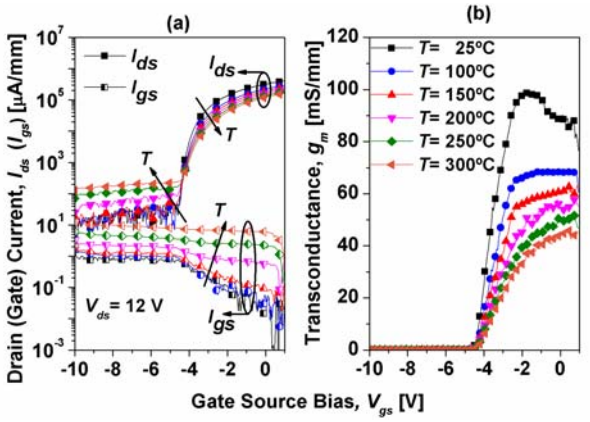

Fig. 1: HEMT drain, gate current and transconductance.

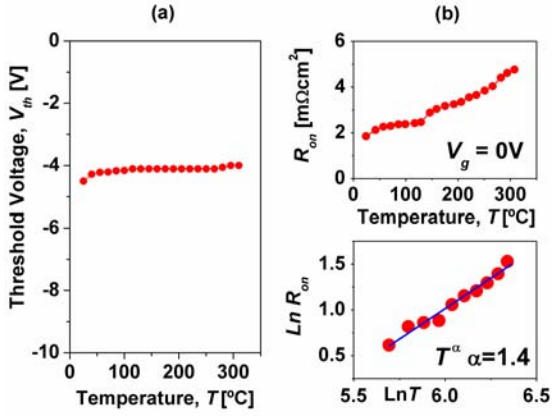

Fig. 2: HEMT (a) threshold voltage, (b) on-resistance *vs T*.

The leakage current (I_{ds}) in the off-state increases with *T*, being in the range of 10-100 µA/mm. Threshold voltage (V_{th}) is remarkably stable in all the temperature range as

it can be seen in Fig. 2(a). I_{ds} decreases with T due to the 2DEG mobility decrease with T (Fig. 1(b)). This result in a degradation of the on-resistance as it is shown in Fig. 2(b). The dependence in temperature has been fitted by a power law as $R_{on} = R_{on,0}\left(T/T_0\right)^{\alpha}$ with T_0=300K and α=1.4. From Fig. 1(a), it can be seen that the gate leakage current (I_{gs}), in the range of 1-10 μA/mm, also increase with the T.

The leakage currents vs T are then analyzed in the configuration shown in Fig. 3, i.e., reverse bias condition. In this study, the reverse bias is in the range of 0-150V which is basically the half of the breakdown voltage of the structure (L_{gs}=L_g=4μm, L_{gd}=5μm). It is worth to mention that neither the GaN buffer nor the AlGaN were not optimized for high voltage operation. For example by the use of AlGaN back barriers, gate dielectric passivation, etc [3], [4], [5].

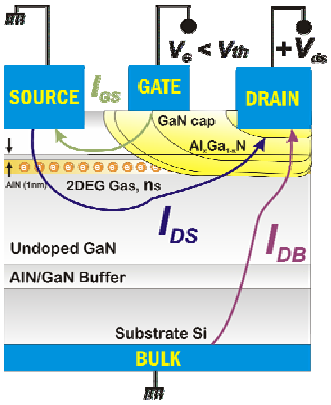

Fig. 3: Reverse bias configuration showing I_{ds}, I_{gs} and I_{db}.

As shown in Fig. 4, the drain reverse current presents a double slope (linear/logarithmic) in their behavior for each T, turning around 75 V of the reverse bias.

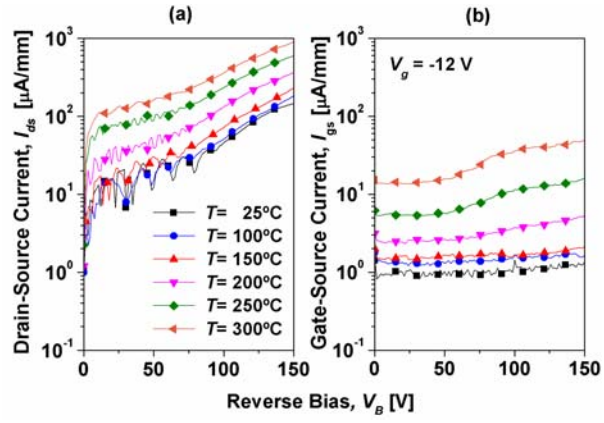

Fig. 4: Drain and Gate reverse leakage current for different temperatures.

Fig. 5 shown the activation energies assuming a rate-limited thermally activated process following an Arrhenius law ($I = I_0 \exp\left[-E_a/k_B T\right]$). Where E_a is the activation energy and k_B is the boltzman constant. From the Arrhenius plot $Ln\left(I_{ds}\right)$ vs $1/T$ the activation energy can be determined. The small the activation energy the more stable is the given phenomenon with the temperature.

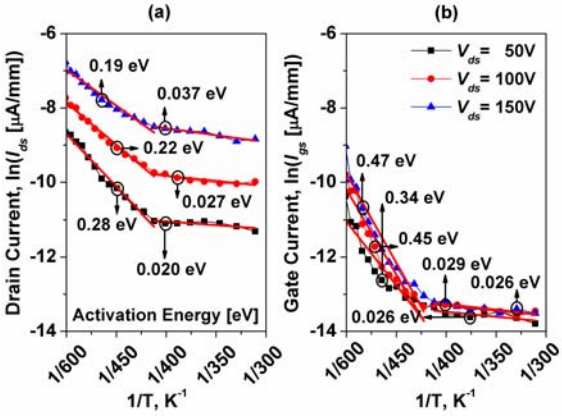

Fig. 5: Arrhenius plot of the drain and gate leakage currents.

As shown in Fig. 4, until 150 °C the leakage current exhibits a weakly increase with T, i.e., E_a ~ 0.02 eV. At higher temperatures, the activation energy is much higher with E_a ~ 0.20 eV and 0.40 eV for drain and gate leakage currents, respectively. These results stress that the elevated temperature could have a relevant impact on the HEMT' reverse currents affecting their reliability despite other transistor parameters, such as V_{th}, are remarkably stable with T.

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EXTRACTION OF THE DEGRADATION PARAMETERS OF CONSTANT VOLTAGE-STRESSED Al/HfYO$_X$/GaAs STRUCTURES WITH IMPORTANT SERIES RESISTANCE EFFECTS

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ABSTRACT

It has been reported several times that the leakage current decay in constant voltage stressed MIS (metal-insulator-semiconductor) capacitors follows the so-called Curie-von Schweidler (CS) dependence $I(t)=at^{-b}$, where I is the current, t is the time and a and b are constants. However, when analyzed in detail the I-t characteristic sometimes exhibit large deviations respect to that expression as occurs for the Al/HfYO$_x$/GaAs structures investigated in this work. It is shown here that the experimental data can be fitted by a phenomenological equation which can be derived from a simple equivalent electrical circuit model. The model is used to evaluate the device degradation parameters associated with the CS dynamics.

1. INTRODUCTION

Compound semiconductors, such as GaAs, are receiving serious attention as the channel material for future CMOS (Complementary-MOS) technology for high speed applications mainly due to the high carrier mobility [1]. However, high-quality and thermodynamically stable gate dielectrics (analogous to SiO_2 in Si CMOS) are still not available for the integration of GaAs substrates in CMOS technology. In addition, for further downscaling of CMOS devices, the conventional gate dielectric, SiO_2, is being replaced by high permittivity (high-k) gate dielectrics, especially HfO_2. The main difficulty for integration of GaAs with high-k gate dielectrics for MOSFET fabrication is the poor quality of the interface between the gate dielectric and the substrate. Towards gate dielectric engineering and mainly to increase the permittivity, incorporation of rare earth elements in high-k dielectrics is being proposed and addition of Y_2O_3 in HfO_2 has been shown to improve the dielectric film quality [2]. Although significant progress has been made in the understanding of the reliability characteristics and degradation mechanisms in Si/high-k stacks, very little information is available in the literature on the reliability issues and breakdown mechanisms in GaAs/high-k systems. It is thus important to study and characterize the degradation mechanisms in GaAs/high-k stacks which are significantly different from Si/high-k systems. In this paper, we present the results of our studies on the degradation behavior of Al/HfYO$_x$/GaAs capacitors. We will consider as a base model the Curie-von Schweidler (CS) law for dielectric degradation [3-5] and show how the deviations from this model can be accounted for using an equivalent circuit representation in which the series resistance plays a fundamental role. The model is ultimately used to extract the degradation parameters associated with the CS law.

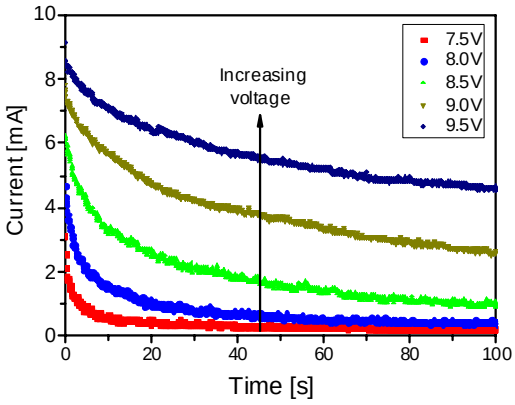

Fig. l: Typical current decay in Al/HfYO$_x$/GaAs structures during constant voltage stress.

2. THE DEVICES

N-type GaAs (100) wafers were used as starting substrate (~1×10^{16} cm^{-3} Te doped). The wafers were first chemically degreased using acetone and isopropanol, cleaned in HCl for 1 minute for native oxide removal and dipped in NH_4OH for elemental As removal. After wet chemical cleaning the samples were dipped into 40% ammonium sulfide $(NH_4)_2S$ solution for 10 minutes to passivate the GaAs surface prior to the deposition of the dielectric. HfYO$_x$ films (t_{ox}≈38 nm, $\varepsilon_{ox}/\varepsilon_o$≈16.4) were deposited by RF magnetron co-sputtering using HfO_2 and Y_2O_3 sputter targets at 100 W RF power in 2.5 mTorr Ar ambient. Post-deposition annealing was carried out in a N_2 ambient at 500 °C for 1 minute by rapid thermal annealing. Al and Au were used as the gate and back electrode, respectively. The measurements were performed at dark conditions and room temperature.

3. EQUIVALENT CIRCUIT MODEL AND PARAMETER EXTRACTION

Figure 1 shows typical *I-t* characteristics measured after a sequence of increasing gate voltages. Although they seemingly follow the decaying function $I(t)=at^{-b}$ associated with CS, when plotted in log-log axes additional features are revealed.

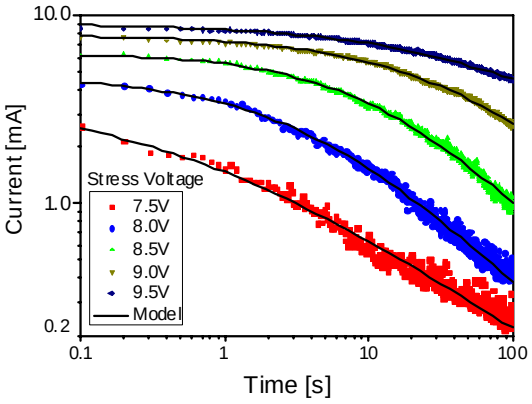

Fig. 2: Typical current decay in Al/HfYO$_x$/GaAs structures during a constant voltage stress.

As shown in Fig. 2, the slopes of the log(*I*)-log(*t*) curves are not constant throughout the degradation process as expected for CS. Interestingly, the experimental data are more properly fitted by the expression:

$$I(t)=\frac{I_0}{1+(t/\tau)^{\beta}} \qquad (1)$$

where I_0 is the initial current, and β and τ are constants. As illustrated in Fig. 3, both models (CS and eq.(1)) are compatible in the long run. Eq.(1) can be rewritten as:

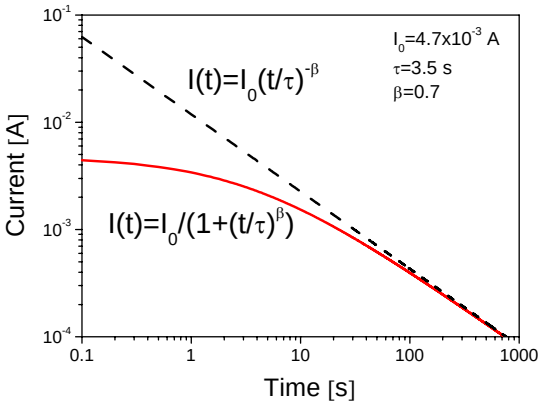

Fig. 3: Comparison between the standard CS model and eq.(1).

$$I(t)=\left(V-I(t)R_S\right)\left[t/\tau^{*}\right]^{-\beta} \qquad (2)$$

where $\tau^{*}=R_S^{-1/\beta}\tau$ and $R_S=V/I_0$. It is worth pointing out that eq.(2) is consistent with an alternative expression for the CS law [6] in which the applied voltage appears as a multiplying factor. Accordingly, eq.(2) is simply the CS dynamics modified by the series resistance effect.

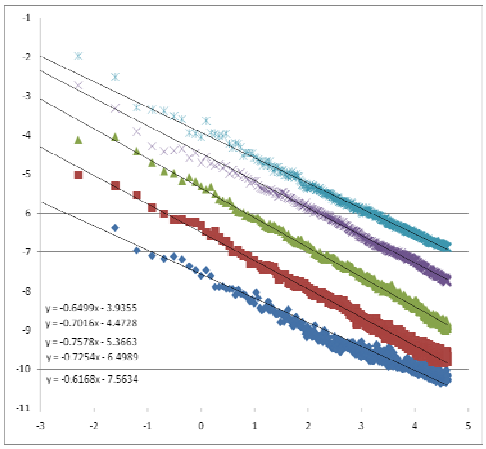

Fig. 4: Data transformation used to extract the model parameters in eq.(3).

Next, eq.(2) can be transformed into:

$$\ln\left[\frac{I}{V-IR_S}\right]=-\beta\ln t+\beta\ln\tau^{*} \qquad (3)$$

so that varying R_S to achieve the minimum linear correlation coefficient (see Fig. 4), the degradation parameters can be extracted (see Table 1).

V [V]	I_0 [A]	τ [s]	β	R_S [Ω]
7.5	2.57E-03	1.99	0.61	2918
8.0	4.71E-03	3.73	0.72	1700
8.5	6.42E-03	11.46	0.75	1325
9.0	7.79E-03	39.98	0.70	1155
9.5	8.64E-03	121.71	0.64	1100

Table 1: Model parameters

4. CONCLUSIONS

Although the model parameters can be directly extracted from eq.(1), eq.(2) provides a more clear picture about the origin of the current deviations observed at the outset of degradation. As illustrated in Table 1 these departures from the CS law can last from a few seconds at the lowest biases to minutes at the highest ones. This has to be taken into account if, as often required in reliability analysis, the injected charge-to-breakdown needs to be computed from the integration of the *I-t* characteristic.

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CHARACTERIZATION OF THE PHASE COMPOSITION AND MICROSTRUCTURE IN DIFFUSION SOLDERED Au/Sn JOINTS FOR DIE ATTACH

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ABSTRACT

The mounting of silicon dice onto copper substrates by isothermal diffusion soldering with the eutectic Au/Sn alloy is demonstrated. X-ray diffraction and scanning electron microscopy are used to identify the intermetallic phases involved in the reaction as well as their microstructure. The Au/Sn solder initially consist of the ζ'-phase and the δ-phase. During the soldering process the binary Au/Sn phases are transformed into a ternary τ_1-phase by a reaction with copper. At short die attach times the reaction is still not complete and parts of the solder remain in the eutectic phase.

1. INTRODUCTION

Recent advances in semiconductor processing towards irregular geometries, high operating temperatures, and ultra thin substrates set high standards for die-leadframe interconnections. [1] Furthermore emerging governmental regulations are restricting the use of lead in electronic assembly. [2] Thus, the development of new joining technologies for the die attach process using lead-free solders is needed.

Isothermal diffusion soldering is a promising technology to achieve thin, reliable and robust joints. [3] It is a mixture of conventional soldering and diffusion bonding, combining the advantages of both traditional methods. In the process a thin layer of solder material is melted on a layer of a high melting point material. By interdiffusion an intermetallic phase is formed in the joint with a melting point significantly higher than the soldering temperature, i.e. the solder is solidified isothermally. The joints produced this way have service temperatures much higher than the fabrication temperature and they can be very thin, thus the time required for reaction is very short.

This work is focused on the characterization of the intermetallic phases involved in the soldering reaction and their microstructure for the eutectic Au/Sn solder on copper leadframes.

2. EXPERIMENTAL

The solder material a 1.1 µm thick layer of the eutectic Au/Sn alloy (80 wt.% Au) was deposited on a 200 mm silicon wafer in an industrial scale sputtering chamber with a deposition rate of 1 µm/min.

For soldering the wafer was cut into square pieces with an edge length of 2.5 mm. These metal coated silicon dice were bonded onto 200 µm thick copper leadframes with a Tresky T-3202 semiautomatic die bonder. For the die attach the leadframes were heated to 330°C under forming gas atmosphere (95 at.% nitrogen, 5 at.% hydrogen). The die was pressed onto the hot substrate with a pressure of 1.5 MPa for 500 ms or 10 s. Thereafter the sample was immediately cooled by pressurized nitrogen.

To simulate the Au/Sn - Cu soldering process in the X-ray diffractometer, Cu was electrodeposited with a thickness of 1 µm on the Au/Sn surface from industrial electrolytes at room temperature and a current density of 3 A/dm². This corresponds to a deposition rate of 0.66 µm/min.

Cross-sections for scanning electron microscopy were embedded in epoxy, mechanically ground and polished. To reveal the microstructure of the layers the samples were additionally ion beam etched for four minutes at 5 kV and a beam angle of 90°. This was done in a Precision Etching Coating system (PECS) from Gatan using Argon as the etching gas. Inspection in the SEM was performed in a Hitachi S4800 with an acceleration voltage of 5kV and a magnification of 30.000x.

For qualitative phase analysis X-ray diffraction was done in a Siemens D501 powder diffractometer in coupled Bragg-Brentano reflection mode with Cu-Kα radiation. The X-ray beam was passed through a graphite monochromator, a soller slit and a 0.05 receiving slit on the secondary side as well as a 1° divergence slit on the primary side. As a detector a scintillation counter with an entrance angle of 0.6° was used. The specimens were mounted symmetrically to the incident and to the diffracted beam. To identify the observed phases, data from the Powder Diffraction File (International Center for Diffraction Data) and the Inorganic Crystal Structure Database (Fachinformationszentrum Karlsruhe) was used.

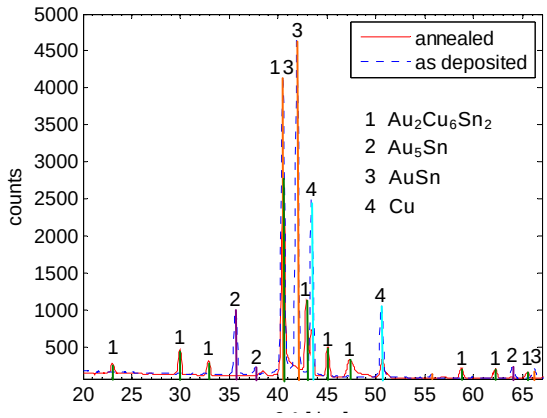

Fig. 1: Detail of the X-ray diffraction spectrograms of the Au/Sn – Cu layer stack as deposited and annealed

3. RESULTS AND DISCUSSION

According to the Au-Sn phase diagram [4] the hexagonal ζ'-phase (Au_5Sn), the hexagonal δ-phase (AuSn), and the orthorhombic ε-phase ($AuSn_2$) are stable at room temperature in the Au/Sn solder layer. Qualitative XRD analysis show that the initial solder layer consists exclusively of the ζ' and the δ-phase (see Figure 1).

Copper is present in its fcc structure. Given these basic conditions, the ratio of ζ' to δ-phase can be determined according to the phase diagram to be 60:40. To simulate the thermal budget the solder joint experiences during die attach the sample is annealed at 330°C for seven minutes. The recorded diffraction pattern is also shown in Figure 1. After this treatment no more of the original Au/Sn phases can be found and the intensity of the copper reflexes is significantly reduced. The original binary phases are transformed into a ternary phase with copper. This τ_1-phase ($Au_2Cu_6Sn_2$) has a primitive cubic unit cell and the crystal structure is of the β-manganese type. [5]

Figure 2 illustrates this phase evolution by SEM micrographs. After a short 500 ms die attach the ternary $Au_2Cu_6Sn_2$ compound as well as the initial solder material, the eutectic mixture of the hexagonal ζ' and δ Au/Sn phases, are present. When the die attach time is prolonged to 10 s all the solder material is transformed into the ternary compound.

If the reaction is not completed during the die attach it still can continue during the operation of the device at temperatures below the melting point of the solder. This reaction in the solid state can cause significant voids in the joint by the Kirkendall effect and result in a failure of the device.[6]

4. CONCLUSION

By X-ray diffraction it was found that the sputtered layer of the eutectic Au/Sn alloy initially consists of the ζ'-phase (Au_5Sn) and the δ-phase (AuSn). Upon reaction with copper during the soldering process both phases are transformed into the ternary $Au_2Cu_6Sn_2$ phase. A die attach time of less than 500 ms leads to an incomplete transformation which can cause Kirkendall voids during the operation of the device.

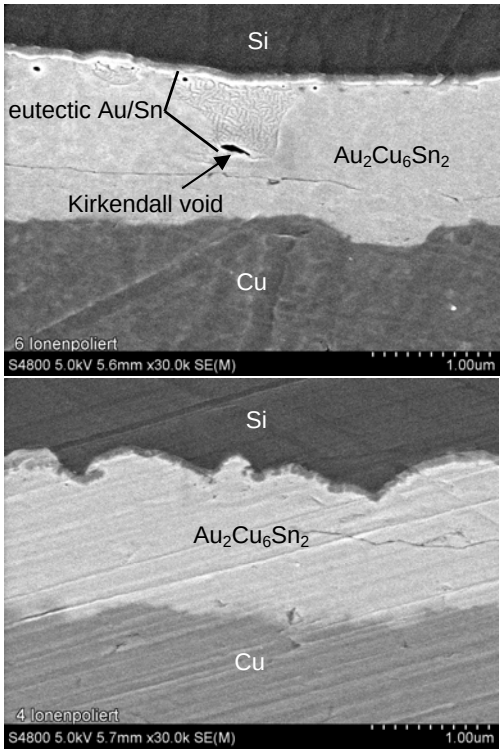

Fig. 2: Scanning electron micrographs of the solder joint. top: 500 ms die attach time. Some of the original eutectic Au/Sn phase has still not reacted with the copper of the leadframe. A Kirkendall void is formed at the interface. Bottom: 10 s die attach. The soldered material has been completely transformed in the final $Au_2Cu_6Sn_2$ phase.

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THERMAL ASSESSMENT OF AlGaN/GaN ON 50µm SILICON MICROSTRIP TECHNOLOGY

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ABSTRACT

Thermal simulations and Load Pull measurements on GaN-on-Silicon discrete devices give the evidence of the better Microstrip technology thermal management, and the related lower junction temperature, with respect to the coplanar solution if a very thin Si substrate thickness is considered. In this paper, the RF power performances variation as function of different Gate-to-Gate pitch and Gate periphery on a 50µm Silicon substrate thickness will be investigate and correlate to the channel temperature and the thermal resistance.

1. INTRODUCTION

Silicon substrates offer low cost and large wafer diameter compared to Silicon Carbide (SiC), but for high power application, SiC is actually the best candidate to have an optimum heat management thanks to the higher thermal conductivity [1]. On the other hand, thermal simulations on GaN/Si epitaxy, considering P_{DISS}=5W/mm with different back temperatures (50 to 80°C), show that Si substrate thinned down to 50µm allows a junction temperature $T_J \leq 150$°C (Fig. 1), which represent a useful working temperature for many power applications.

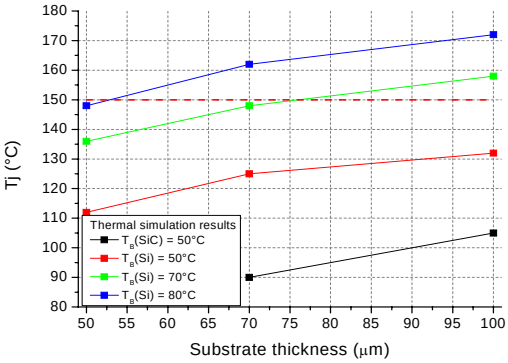

Fig. 1: Junction Temperature versus substrate thickness and back temperature.

Experimental results collected on GaN/Si Microstrip (MS) device give the evidence of better power performances with respect to Coplanar (CPW) technology, related to the better thermal management.

To further optimise thermal performances of MS device, in this work we will evaluate the output power density and device channel temperature for different layout geometry, where we will highlight the thermal effect related to different Gate-to-Gate pitch by infrared thermography technique adopting a camera based set-up [2]. Average channel temperature has also extracted and correlated to the maximum RF power performances for the analysed device.

2. DEVICE FABRICATION

The active devices reported in this work have been fabricated with the SELEX Sistemi Integrati GaN-HEMT MS technology. This procedure, optimized on Silicon Carbide (SiC) substrates, has been applied on the AlGaN/GaN heterojunction grown on a highly resistive (ρ = 6 kΩ·cm) 4 inches Si (111) substrate, where the ohmic contact procedure optimization has been mandatory because of the different Silicon thermal behaviour during the Rapid Thermal Annealing (RTA), yielding a contact resistance of about R_C=0.25Ω·mm with a Ti/Al/Ni/Au metallization.

A further backside process optimization has been performed for Si MS technology, lapping down to 55µm by an abrasive 9µm Alumina dust followed by a polishing treatment to make easier the mask alignment for via-holes lithography. ICP etch process and RIE Chlorine plasma have been optimized for Silicon via holes formation and GaN buffer etch to reach the front metal, followed by the backside metallization to achieve the ground reference. This optimized process allows to completing the Si backside in half time with respect to the SiC one.

3. THERMAL AND POWER PERFORMANCES

To emphasize thermal effects related to an increasing PRF (Pulse Repetition Frequency) on the RF power performance, an extensive source/load-pull campaign has been exploited on a W_G=1mm (10x100µm) FET, comparing CPW and MS technologies on two wafer with a comparable epitaxy. Such measurements are performed in pulsed condition through pulse duration of 20µs and a Duty Cycle ranging from 1% to 50% with 25°C of backside temperature. The nonlinear characterization has been performed at 3GHz with a pulsed Drain Bias of 25V and I_{DS}=30%I_{DSS}. P_{OUT} and PAE are evaluated at 3dB of Gain compression, varying duty cycle as illustrated in Fig. 2. Such data show that increasing duty cycle the CPW devices power performance gives a 20% reduction of Drain current, compared to 5% of MS devices. This phenomenon could be explained in reason of the thicker substrate, where thermal conductivity is lower and a

higher junction temperature is generated by increasing Duty Cycle.

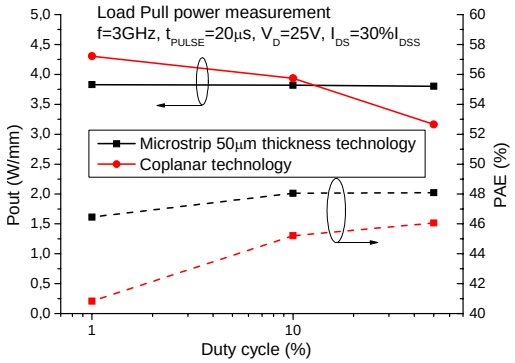

Fig. 2: POUT and PAE performance @ 3dB Gain compression (CPW and MS technologies).

To better evaluate MS FET performance with respect to W_G, the pulse duration and Duty Cycle have been fixed respectively at 20µs and 50%. In said condition, a FET family 10x with different Gate finger widths, from 75µm to 200µm, has been characterized in terms of saturated output power density as can be depicted in Fig.3.

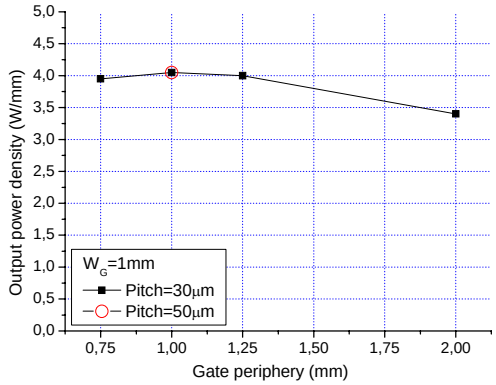

Fig. 3: P_{OUT} related to W_G of 10x family: black line (10x family, 30µm pitch), red circle (W_G =1mm, 50µm pitch).

Results show that output power density is unvarying with respect to Gate widths up to a finger of 125µm. Increasing Gate width up to 200µm, RF output power density decreases of about 0.6 W/mm due to thermal phenomena, while no output power variation is appreciable varying Gate-to-Gate pitch from 30µm to 50µm on the W_G=1mm device, upon which the effective thermal capability has been investigated by means of IR thermal measurements.

In Fig. 4 are reported the mean junction temperatures evaluated at three different power dissipation on two devices with 30µm and 50µm Gate-to-Gate pitch. Thermal resistance has also been extracted in both cases, with device back temperature fixed at 70°C. As we expect, the mean junction temperature is slightly lower for the 50µm case, due to the lower thermal interplay between different Gate fingers. These results show that for 30µm Gate-to-Gate pitch case, a maximum junction temperature of 138°C is expected for back temperature of 70°C in agreement with simulations, and 132°C if 50µm pitch is considered.

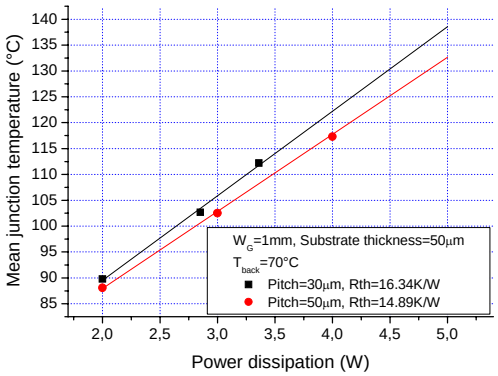

Fig. 4: Mean temperature junction vs. power dissipation for two different Gate-to-Gate pitch.

Fig. 5 shows temperature increase normalized to 3W power dissipation obtained on the tested devices. In both cases, temperature distribution on the active area is quite uniform: no particular evidence of current constriction is visible.

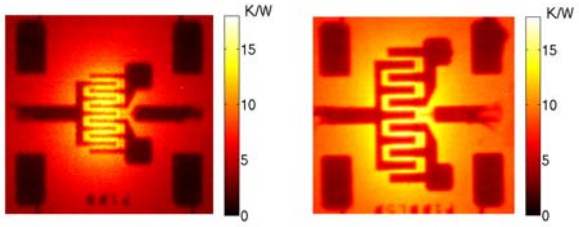

Fig. 5: Temperature increase normalized to 3W power dissipation on 30µm (left) and 50µm (right) Gate-to-Gate pitch devices.

4. CONCLUSIONS

According to thermal simulation, GaN-on-Si Microstrip devices have been fabricated in order to obtain a junction temperature reduction.

Load Pull power measurements, obtained with a duty cycle ranging from 1% to 50%, show a 20% output power reduction on CPW devices, instead of 5% observed on MS ones. Considering the worst 50% duty cycle condition, a constant output power density of 4W/mm is appreciable up to 125µm Gate finger width, while a power density reduction of about 0.6 W/mm can be observed only when 2mm Gate periphery is considered, due to thermal phenomena. Infrared thermal measurement confirm the good agreement with simulation data, and show that increasing the Gate-to-Gate pitch gives a little mean thermal resistance reduction, and consequently a lower mean junction temperature, on equal output power density.

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LARGE SIGNAL OPERATION OF InAlN/GaN HEMTs AT VERY HIGH TEMPERATURE

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During the last years InAlN/GaN has been emerged as a material for high electron mobility transitors (HEMTS). Its high ceramic-like stability, the absence of mechanical stress in the heterojunction in its lattice matched configuration and its high interfacial sheet-carrier density of N_S = 2.8 x 10^{13} cm^{-2} 0 makes it a promising candidate for reliable high temperature operation. As demonstrated in inital short time operation at 1000 °C in vacuum 0. It has shown to be high temperature stable up to 250 hrs at 800 °C without degrading the heterostructure and showed 50 hrs of operation at 900 °C where electromigration of the gate was limiting the device lifetime 0. Here we will report on first 1 MHz large signal measurements at 1000 °C (in vacuum).

The device was fabricated from MOCVD grown InAlN/GaN on sapphire with a barrier thickness of 12 nm. Device insulation was achieved by argon based dry mesa etching. The ohmic contacts where annealed at 800 °C. Device passivation is 30 nm of Si_3N_4. The gate input voltage V_{GS} was between the device pinch-off voltage (~-2 V) and +1 V. The maximum drain source voltage was V_{DS} = 10 V. Testing has been by needle probes since no other method of contact has been available.

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MITIGATION OF HOT-PHONON EFFECTS IN A TWIN-CHANNEL NITRIDE HETEROSTRUCTURE FIELD EFFECT TRANSISTOR

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ABSTRACT

Lifetime of non-equilibrium (hot) longitudinal optical phonons is measured in a twin channel confined in an $Al_{0.82}In_{0.18}N/AlN/Al_{0.1}Ga_{0.9}N/GaN$ heterostructure where the mobile electrons form a camelback-like density profile at high electric fields. The lifetime is found to depend on the shape of the profile rather than solely on the electron sheet density. A shorter hot-phonon lifetime is demonstrated as compared with that in a standard design. This allows one to increase the sheet density without any deleterious effect on the lifetime. The measured hot-phonon lifetime is below ~60 fs at hot-electron temperatures of 600 K when the sheet electron density is $1.8\cdot10^{13}$ cm^{-2}.

1. INTRODUCTION

Gallium nitride heterostructure field-effect transistors are promising for applications at microwave and millimeter wave frequencies [1-3]. The main drawback is a steep reduction of the power as the frequency increases. It is expected that more power can be processed and the capacitances can be charged faster if more electrons are present in the channel. The highest electron sheet densities (over $3\cdot10^{13}$ cm^{-2}) are achieved in GaN channels when an InAlN barrier is used together with an AlN spacer [4]. However, the decay of non-equilibrium (hot) phonons is relatively slow and the electron drift velocity is low at high electron densities [5,6]. This forces one to consider designs where a higher electron sheet density is combined with a wider electron density profile [7].

The hot-phonon decay is the fastest near the plasmon–LO-phonon resonance [8]. Correspondingly, the electron drift velocity is the highest at the resonance density if the same electric field is applied along the channel [6,9]. For standard voltage biased GaN-based channels, the resonance density is near ~$1\cdot10^{13}$ cm^{-2}. Thus, no benefit from the plasmon–phonon resonance is obtained for the highest achievable densities. The twin channel design has been proposed in order to increase the resonance sheet density [7]. The paper aims to demonstrate the possibility to combine high values of sheet electron density (prerequisite for power operation) and fast decay of hot phonons (useful for fast operation) in an $Al_{0.82}In_{0.18}N/AlN/Al_xGa_{1-x}N/GaN$ structure with a composite $Al_xGa_{1-x}N/GaN$(x<0.2) channel.

2. ELECTRON DENSITY PROFILE

Solutions of coupled Schrödinger–Poisson equations are illustrated in Fig. 1 for a reference structure (dashed line) and $Al_{0.82}In_{0.18}N/AlN/Al_{0.2}Ga_{0.8}N/GaN$ structure (solid lines). The $Al_{0.2}Ga_{0.8}N$ interlayer causes a shoulder to appear next to the main peak. The shoulder grows, and eventually a camelback profile develops at elevated hot-electron temperatures. For the same peak density, the electron sheet density can be increased from $1\cdot10^{13}$ cm^{-2} (Fig. 1, dotted line) to the values above $2\cdot10^{13}$ cm^{-2} at electron temperatures above 1000 K (solid lines).

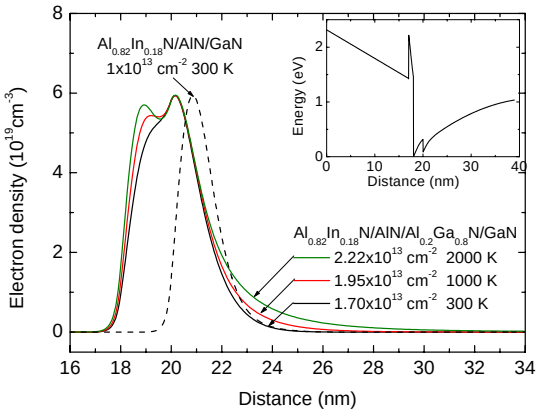

Fig. 1: Calculated electron density profiles at different hot-electron temperatures. Inset illustrates the band diagram for the camelback design.

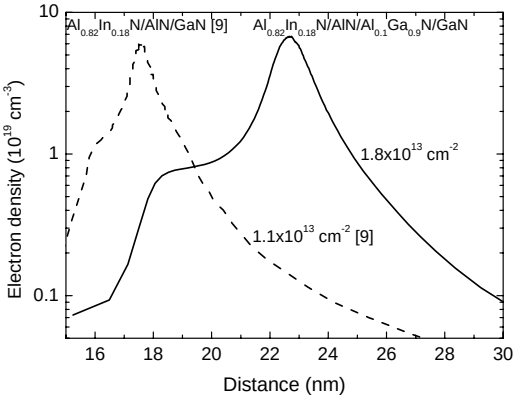

Fig. 2: Electron density profile in a standard AlInN/AlN/GaN heterostructure (dashed line, [9]) and twin-channel design $Al_{0.82}In_{0.18}N/AlN/Al_{0.1}Ga_{0.9}N/GaN$ (solid line, present paper).

The experimental study was carried out on nominally undoped $Al_{0.82}In_{0.18}N/AlN/Al_{0.1}Ga_{0.9}N/GaN$ structure grown in a vertical low-pressure metal-organic chemical vapor deposition (MOCVD) system. The structure consisted of a GaN buffer layer, a 3-nm $Al_{0.1}Ga_{0.9}N$ interlayer, a 1-nm pseudomorphic AlN spacer, and an AlInN barrier. Schottky diodes were formed for density profile measurements.

Solid line in Fig. 2 illustrates that the electrons are mainly located in the GaN layer (z>21 nm), but some electrons occupy the $Al_{0.1}Ga_{0.9}N$ interlayer. The predicted shoulder is found at 18<z<21 nm. The sheet electron density is considerably higher in the novel design (solid line) when the peak densities per unit volume are comparable.

3. HOT-PHONON LIFETIME

The hot-electron fluctuation technique is the most suitable way for measuring the dependence of hot-phonon lifetime on supplied electric power [10]. In order to avoid effects of heat accumulation by acoustic phonons, short pulses of voltage are applied to a gateless 2DEG channel, and a gated modulation-type X-band radiometer is used for measuring the noise temperature of hot electrons. Because of the dominant energy exchange between the hot-electrons and the hot-phonons, the quasi-equilibrium state is reached among them, and thus the noise temperature, the hot-electron temperature, and the equivalent hot-phonon temperature are nearly equal. The dependence of the hot-phonon lifetime on the hot-electron temperature is illustrated in Fig. 3.

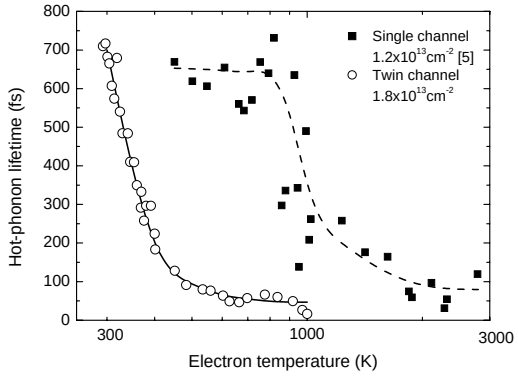

Fig.3: Dependence of hot-phonon lifetime on hot-electron temperature in AlInN/AlN/GaN (squares, [5]) and the novel twin channel (circles, present paper). Curves guide the eye.

Despite essentially different sheet electron densities, similar values for the hot-phonon lifetime are obtained when the heating is weak (circles and squares). However, the lifetimes decrease at different rates as the temperature increases, and the camelback design demonstrates several times faster decay of hot phonons at the elevated hot-electron temperatures. Thus, the novel design combines the highly desirable high sheet density with the ultrafast decay of the hot phonons at elevated hot-electron temperatures.

4. CONCLUSIONS

The hot-phonon decay lifetime is estimated from experiment for $Al_{0.82}In_{0.18}N/AlN/Al_{0.1}Ga_{0.9}N/GaN$ heterostructure where the mobile electrons are spread in the composite $Al_{0.1}Ga_{0.9}N/GaN$ channel and form a camelback electron density profile at high electric fields. In accordance with the expectation, the parameter of importance for the lifetime is not the total charge in the channel (the electron sheet density) but rather the electron density profile. This is demonstrated by comparing two structures with similar peak electron density per unit volume (~$6\cdot10^{19}$ cm^{-3}) but with different density profiles. The camelback profile supports a faster decay of hot phonons as compared to the decay in a standard single-channel heterostructure.

ACKNOWLEDGMENT

This work is supported by grants FA8655-09-1-3103 and FA9550-04-1-04-14 from the US Air Force Office of Scientific Research under the direction of Dr. Kitt Reinhardt. Postdoctoral fellowship for E.Š. is being funded by European Union Structural Funds project "Postdoctoral Fellowship Implementation in Lithuania"

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Session 6 :

Challenges and perspectives

Chair : Prof. Petra Specht

Tuesday May 31, 09:00 - 09:40

CONFERENCE REPORT: 47TH WORKSHOP ON COMPOUND SEMICONDUCTOR MATERIALS AND DEVICES (WOCSEMMAD 2011)

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ABSTRACT

The aim of this paper is to make a brief review of the last WOCSEMMAD 2011. After a presentation of the workshop focus and scope, a selection of novel interesting results will be presented.

1. INTRODUCTION

The Workshop on Compound Semiconductor Materials and Devices was launched by Prof Lester Eastman (Cornell University) in 1964 who attended the first 45 events. Its focus is mainly on III-V electronic and optoelectronic devices. It has paved the way of all the compound semiconductor device history and gathers a small community of scientists invited to come and discuss together. The participation is possible on invitation only. The attendance is mainly American oriented however international participants are welcome. This conference is a place in which open discussions are welcome, not to say mandatory. The fact that no written documents are required facilitates informal talks. This is also due to the limited number of attendees (about 75).

This conference is very important to research teams to get funding from administrations (mostly DoD). Four DoD representatives were present during a specific rump session.

Other attracting elements make this conference a very stimulating place. A panel session is devoted to a specific topic each year and a beer bet session is devoted to predictions of possible breakthroughs for the next year. Last but not least the conference always takes place in a lovely place despite the winter season where it is scheduled (3rd week of February).

2. GaN ELECTRONICS

The activity on GaN materials and devices remains important and concerned the most part of the workshop. The European visibility is quite good especially in the field of InAlN HEMTs. In future the conference scope will outreach to new topics and applications such as: organic electronics, nanowires, THz, etc.

In the frame of AlInN/GaN devices, ARL presented important trade off of material and thicknesses of passivation dielectric to reduce parasitic capacitances for very high frequency operation, while ULM University presented InAlN HEMTs with submicron buffer for better thermal management. University of Wien presented InAlN thin barrier E-mode devices with ALD deposited gate oxide showing very low gate leakage current, Finally, also University of Notre Dame presents their recent progress on InAlN HEMTs with ultra-thin AlN barrier, where Ft of 219 GHz has been demonstrated on MBE regrown ohmic contacts.

Concerning GaN HEMTs, NRL presented an Ultra-Thin Barrier AlN/GaN HEMTs Grown on Free-Standing HVPE GaN Substrates, demonstrating the presence of a double channel. Interestingly the upper channel can act as a screening layer for surface traps. NRL have also presented the high frequency properties of the GaN MISHEMTs. Finally Chalmers presented Thin-barrier AlGaN/AlN/GaN HEMTs with 50% Al content achieving high sheet density and room-temperature mobility.

Reliability data on GaN and InAlN HEMTs has also been presented. III-V labs presented preliminary reliability data on InAlN HEMTs. Interesting reliability investigation with device simulation and correlation between RF and DC degradation has been presented by U.S. Navy Postgraduate School. The University of Padova Group also presented reliability data in devices with different substrates and provided preliminary correlation data with electroluminescence.

3. TUNNELING IN COMPOUND SEMIC.

A special session on Tunneling compound semiconductors has been organized. Penn State University presented Tunnel Transistors for Logic and Memory achieving steep slope transistor and highlighting the D_{it} as the main limiting factor. University of Minnesota presented Si tunneling FETs; they demonstrate tunneling in Si/SiGe material system and pointing out that Si/SiGe allow staggered bands alignment achieved with the advantage of utilizing CMOS compatible process. Ohio state University have shown that it is possible to have tunneling effects in GaN while University of Notre Dame has presented a new InAs/AlGaSb vertical TFETs (vTFET) device.

4. DIAMOND ELECTRONICS

Some activity on Diamond either in Europe as well as in Europe has been presented. Cornell demonstrated regrowth on GaN bonded to diamond is possible without any buried charge at the etched interface. This enables any GaN based structure to be grown including AlInN, thin AlGaN, AlN interbarrier. ULM University also presented results in Diamond on GaN technology for better thermal management.

4. NOVEL MATERIALS AND GROWTH

Chris Palmstrom from UCSB showed very interesting self-organization of ErAs nanorods in GaAs. Those nanorods are regularly located within the GaAs matrix. One interest of those ErAs compounds could be in their excellent thermoelectric properties with improved capability to extract power from a temperature gradient thanks to improved Seebeck coefficient.

Alan Doolittle from Georgia Institute of Technology presented their work on the growth of single phase InGaN throughout the immiscibility gap. The growth of single phase

InGaN was obtained by avoiding In surface segregation. This is achieved using their Metal-Modulated Epitaxy (MME) based on Molecular Beam Epitaxy. The principle is to use a pulse-like indium metal deposition followed by GaN capping. The growth temperature was set in the 400°C to 450°C range.

Wayne Johnson from Kopin Corporation presented recent work on the growth of InAlN/GaN heterostructures. They observed that Ga-free contamination in InAlN materials lead to higher sheet resistances. By adding 4% of Ga in the $In_{13\%}AlN$ film, the sheet resistance dropped by about 20%, i.e. from 228 Ω per square down to 180 Ω per square. Two opposite mechanisms seemed to operate: increase of the electron mobility from 1150 to 1550 $cm^2\ V^{-1}\ s^{-1}$ and a slight decrease of the 2 dimensional gas density. The influence of the Ga controlled content in the InAlN structure was not yet understood.

UC Berkeley contributed with the formation of laterally grown GaAs / dilute nitride QWs, achieved without Au seeding on silicon substrates and a novel TEM sample preparation technique featuring electron transparent needles with atomically clean surfaces. The preparation technique is principally applicable to all materials.

Alan Seabaugh from the University of Notre-Dame presented outstanding results on III-V Tunnel FETs using InAs(n-type)/AlGaSb(p-type) heterojunction. The very original approach is based on 3-D structure with the use of semiconductor bridges.

5. MATERIALS & DEVICE CHARACTERIZATION

The characterization session was dominated by transmission electron microscopy analysis. Arizona State University presented mapping of spontaneous and piezoelectric fields by electron holography in nm resolution. Contributions from Berkeley, LBNL and UCB, showed current progress utilizing aberration-corrected TEM. Low voltage, low dose microscopy was introduced which allows to image features commonly not accessible with TEM such as weekly bonded atoms at nanocluster surfaces. Ohio State University presented an overview on defects and their energy positions in the bandgap of group III – nitride alloys.

6. OPTOELECTRONICS

Two very interesting sessions on optoelectronics has also been given, dealing with UV emitters (designing structures with much higher efficiency), as well as with $In_{0.5}Ga_{0.5}As$ quantum dot light emitters on GaP for optoelectronics on Si (from Yale University). Droop and Green Gap has also been largely debated. Finally an Hybrid III-Nitrides/SiC Ultraviolet Avalanche Photodiodes has also been presented by U.S. Army Research Laboratory.

7. PANEL DISCUSSION

This is a major event of this conference because it gives insights on the DoD future compound semiconductor research directions. This year's panelists were: Dan Green (ONR), Pani Varanasi (ARO), Laura Rea (WPAFB). Don Silversmith (DTRA) Further information on the specific programs those program managers are funding is available on the DoD website

Within the WOCSEMMAD community usually contributions to basic research programs are asked for when the panelists are giving their comprehensive overviews. Emphasis is on innovative, groundbreaking new ideas which have a long-term relevance to DoD programs. Some research areas of interest for the participating agencies are:

- Power and Energy Research (ARO)
- Defect Science and Engineering (ARO)
- Freestanding novel materials beyond graphene (ARO)
- GaN EM program (ONR)
- ALD fundamental study of III-Vs (ONR)
- Phase transition materials (ONR)
- Metamaterials (WPAFB)
- Photonics Monolithic Integration (WPAFB)
- Radiation effects of various materials (DTRA)

Response from the audience is often guided by issues for concrete funding. A more general discussion arose on the value of publishing in specific journals, how funding agencies view publication records and the often detrimental effect publishing in non-scientific papers can have on serious research efforts. As an example the public "hype" about cloaking techniques with negative index materials was discussed.

8. MOST VALUABLE CONTRIBUTION AWARD

Each year the workshop ends by the presentation of the Most Valuable Contribution Award, which was attributed in 2011 to Petra Specht (Berkeley Univ.) for her contribution "*The effect of electron irradiation on TEM investigations*" and also contribution to questions and answers throughout the workshop.

ACKNOWLEDGEMENTS

The authors thank Shari Allwood for her great support on the WOCSEMMAD organization.

GaN AND SiC FROM INDUSTRIAL PERSPECTIVES

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Energy management, from production, distribution, conversion up to the final usage is becoming one of the most interesting fields in terms of research, development and business.

On top of classical silicon based devices, wide band-gap materials are collecting more and more interest. Wide effort has been put in place in optimizing the bulk substrate, in solving several technical issues and finally in demonstrating working devices able to optimize energy efficiency in several applications.

On top of SiC and GaN diodes switches are starting to appear on the market and enthusiastic forecast in the Billion dollar range are provided for market in 2020.

The talk will analyze the limits, the needs and the possibilities to make it happen trying to set a right positioning in the application scenario of the forecasted products as well as discussing the limiting factors and the potential developments from an industrial perspective.

Finally some results from the program LAST POWER will be reported as it is implementing an industrial strategy for 6" SiC and GaN on Silicon roadmaps.

The LAST POWER project has received funding from the ENIAC Joint Undertaking under grant agreement n° 120218 and from the national programs/funding authorities of Greece, Italy, Poland, and Sweden.

Session 7 :

Nitrides : materials and processing

Chair : Prof. Takashi Mizutani

Tuesday May 31, 09:40 - 11:00

INFLUENCE OF SUBSTRATE MISCUT ON PROPERTIES OF GaN-BASED DEVICES

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ABSTRACT

The work shows an influence of GaN substrate misorientation on the AlGaN and InGaN layers used in such electronic devices as laser diodes and high electron mobility transistors. The following effects have been experimentally verified: i) higher efficiency in p-doping, ii) better morphology of the layers, iii) trigonal deformation of unit cells, iv) less problems with cracking- higher critical thickness and Al-content in AlGaN layers, v) smaller incorporation of indium into InGaN layers. All those findings should be taken into account when designing the epi-structure on the off-axis substrates for GaN-based devices.

1. INTRODUCTION

In heteroepitaxy, miscut substrates are typically used to obtain the desired morphological, optical and electrical properties. Usually, this tilt is around 1 degree, however, in some cases, much bigger tilt is an optimum. For example, in SiC epitaxy, 4-degree-off or even 8-degree-off substrates are used.
In the case of GaN epitaxy, the experimental data on that issue is very limited [1-5]

The aim of this paper is to summarize all effects observed experimentally for AlGaN and InGaN layers grown on misoriented GaN substrates. Most of the layers were grown using MOVPE (metalorganic vapour phase epitaxy), but so far we have not observed any significant differences (concerning the influence of GaN substarte misorientation) when the layers were grown using MBE (molecular beam epitaxy)

2. MORPHOLOGY

Fig. 1 shows morphology of the GaN layer grown on non-misoriented GaN substrate. It can be seen that each dislocation (here, at density of 10^5 cm^{-2}) produces a hillock what is detrimental in technology of such devices as laser diodes or high electron mobility transistors (HEMTs).
It is possible to avoid formation of such hillocks by using the GaN substrates of misorientation between 0.5 and 1 degree. In such a case, the growth of GaN layer is via the step flow, what can be seen in Fig.2 showing the AFM (atomic force microscopy) scan with straight monoatomic steps.

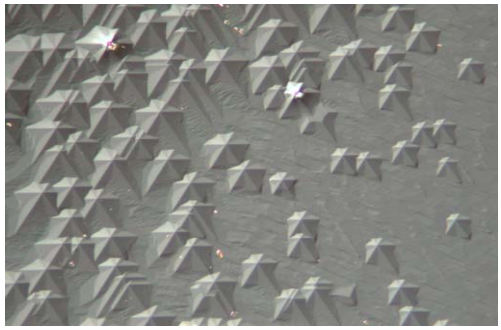

Fig. 1: Nomarski topograph of the GaN layer surface after growth on non-misoriented GaN substrate. Each hillock has a size of about 30 microns.

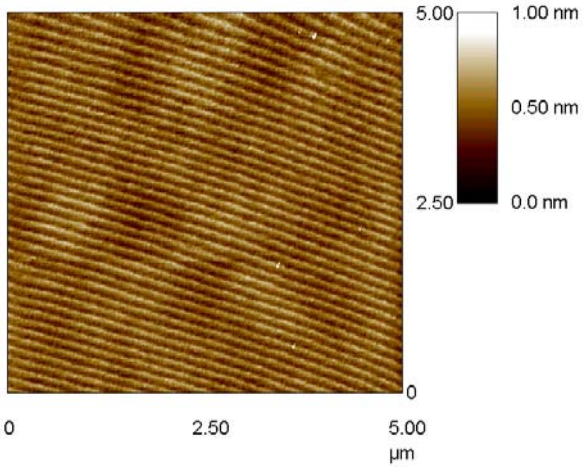

Fig. 2: AFM topograph of GaN MOVPE layer grown on GaN bulk substrate with misorientation of 0.6 degree.

For higher misorientations, above about 1 degree, the morphology gets worse because of step condensation and bunching.

3. P-DOPING

Fig. 3 shows a dependence of a hole concentration in GaN:Mg MOVPE layers versus substrate misorientation. It can be seen that it is advantageous to use misoriented GaN substrates [4]. SIMS (secondary ion mass spectroscopy) showed that magnesium concentration in both cases is the same. This means that the higher hole concentration is a result of smaller acceptor compensation by native defects, for example, nitrogen vacancies.

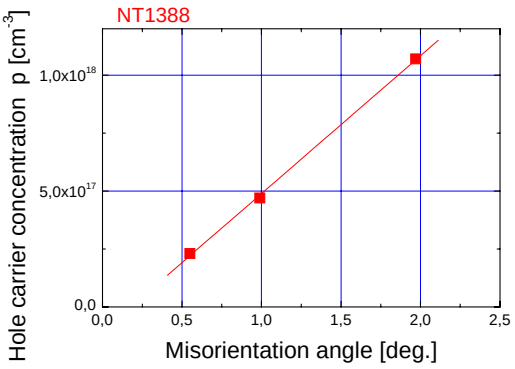

Fig. 3: Hole concentration in GaN:Mg layer versus GaN substrate misorientation.

4. UNIT CELL DEFORMATION

Fig. 4a and 4b show the schematic difference between deformation of unit cells of mismatched epi layers grown on on-axis and off-axis substrates.

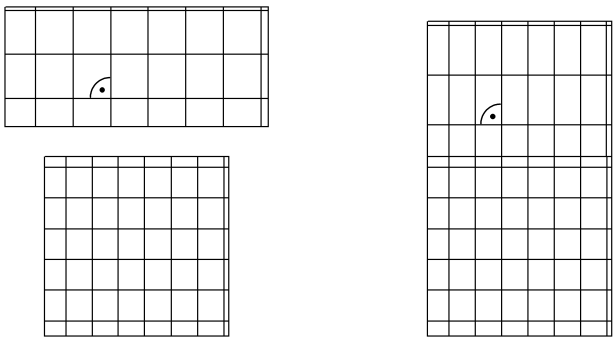

Fig. 4a: Unit cell tetragonal deformation of the mismatched epi layer grown on on-axis substrate

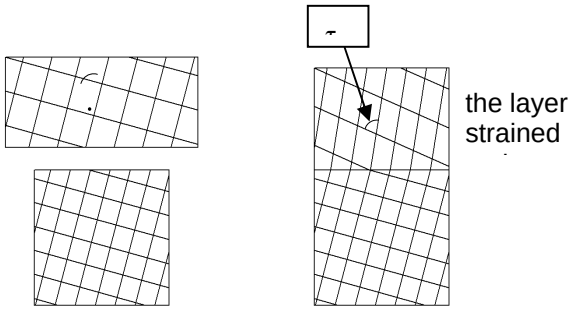

Fig. 4b: Trigonal deformation of unit cells of mismatched epi layers on off-axis substrate.

It can be seen that in the second case, the layers are trigonally deformed, without preserving the angles of 90 degrees. We have calculated the theoretical values for the InGaN and AlGaN layers and we compared those with the experimental data. Table I shows these results. Surpriznglly, the deformation of the unit cells is higher than expected. The origin of this fact is not understood yet.

Layer	Substrate misorient. (degrees)	Theoretical deviation from 90 deg	Experimental deviation from 90 deg
InGaN 20%	0.4	0.031	0.039
20%	0.8	0.053	0.127
17%	1	0.079	0.168
15%	0.6	0.035	0.057
AlGaN 11%	2.1	0.018	0.025
11%	1.8	0.015	0.024

Table 1: Deviation from the 90 degree angle in the unit cells of the epi layers grown on off-axis substrates.

5. CRACKING

AlGaN layers are used in blue and violet laser diodes as cladding layers and in HEMTs for 2-dimensional electron gas (2DEG) formation. In both cases, it is advantageous to have a high aluminum content in those AlGaN layers. Unfortunately, the tensile strain causes layer cracking detrimental for any device construction.

We found that the application of the misoriented GaN substrates helps in avoiding AlGaN cracking. Table II shows the density of cracks for the layers grown in the same growth runs but on differently misoriented GaN substrates.

Sample	Layer thickness [μm]	Crack density δ=0.5 deg [1/cm]	Crack density δ=2.0 deg [1/cm]
Pair A	0.5	5.7	4.0
Pair B	0.75	29	12
Pair C	1.0	24	15

Table 2: Crack density of AlGaN layers grown on c plane equal thickness bulk GaN substrates with different miscut δ off the c axis.

6. INDIUM INCORPORATION INTO InGaN LAYERS

Indium incorporation into InGaN layer depends on the following parameters:

i) growth temperature- for higher temperature, less indium is incorporated,
ii) indium (TMIn in MOVPE) flow,
iii) growth rate controlled by TEGa flow.

The third parameter is not obvious, as we increase Ga flow, but more indium into the ternary compound InGaN is incorporated. This phenomenon occurs only at relatively high temperature and when the growth is via step-flow. The qualitative explanation is based on the fact, that gallium atoms are incorporated at almost 100%, but indium in about 5%, only in the situation, when indium is attached to the atomic step and surrounded quickly by stable gallium atoms.

We deal with a similar case when the growth is on the off-axis or on-axis GaN substrate. As the growth rate in vertical direction does not depend on misorientation, this means that the steps flow faster in the case of on-axis or small substrate misorientation. Fig. 5 shows a dependence of indium content in InGaN layers grown on differently misoriented substrates [5].

It can be seen that for higher misorientation less indium is incorporated, what makes fabrication of the true-blue and green emitters on off-axis GaN substrates more difficult. Moreover, this phenomenon leads to an additional mechanism of indium segregation when the atomic steps are not identical and straight. In the case of InGaN layers grown at relatively low temperatures, morphology is usually bad (the steps are not straight) and therefore, the layers are not uniform.

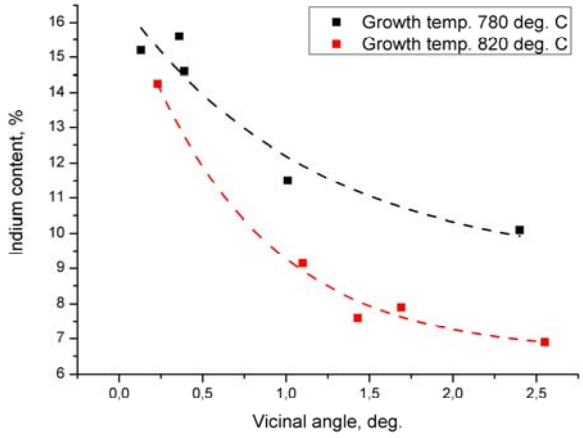

Fig. 5: Dependence of indium incorporation into InGaN layers versus the GaN substrate misorientation for two different growth temperatures.

7. MULTICOLOR ARRAYS OF LASER DIODES

The phenomenon described above of a lower indium incorporation into InGaN layers when grown on an off-axis GaN substrate, is practically used in fabrication of multicolor arrays.

Fig. 6 shows an idea of this approach. By lateral patterning with photolithography and reactive ion etching we can fabricate stripes of different local misorientation.

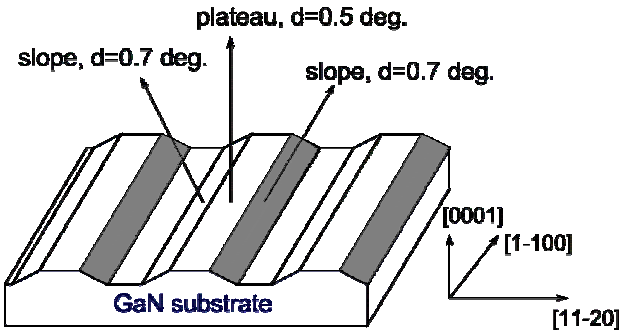

Fig. 6: Idea of fabrication of the laterally patterned GaN substrate to obtain a variable crystallographic misorientation across the wafer.

Onto such laterally patterned GaN substrate we deposited laser epi-structure and we optically pumped to obtain lasing. Fig. 7 shows the positions of the peaks from two areas which were differently misoriented. This results proves a feasibility of such approach and will be the base for fabricating electrically pumped multicolor arrays.

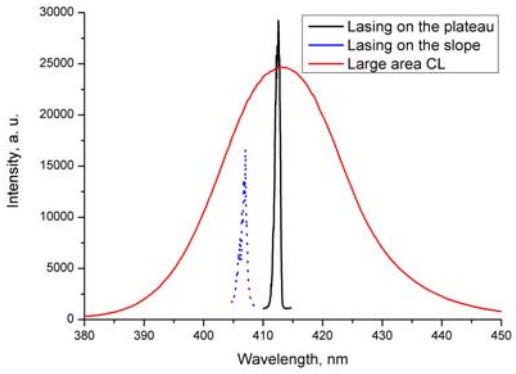

Fig. 7: Lasing spectra of a test structure with 5 InGaN/GaN QW grown on the undulated GaN substrate, obtained by optical pumping in the slope and plateau regions. In the slope the lasing wavelength is 407 nm, and in the plateau it is 412 nm. Also shown is a cathodoluminescence spectrum acquired from large area of the sample covering both the slope and the plateau regions

8. CONCLUSIONS

We have presented the main effects accompanying the growth of ternary layers of AlGaN and InGaN on mismatched and misoriented GaN substrates. The of substrate misorientation effects include:

- improvement of morphology of all layers,
- more efficient p-doping
- less cracks in AlGaN layers
- unit cell trigonal deformation
- smaller indium incorporation into InGaN layers.

The experimental results shown were obtained for the bulk GaN substrates, however, similar results we have for sapphire and SiC substrates. For those two substrates, the (AlGaIn)N layers are of high crystallographic quality (however, much worse than for the GaN substrates). For Si substrates, which gives worse crystallographic quality, the results are not the same and are under current evaluation.

An interesting option of technology is a monolithical integration of SiC power transistors and GaN-based devices, both grown on SiC substrates. Up to now, SiC epiataxy used 8 and 4 degree misorientation, and GaN devices are usually grown on on-axis sapphire substrates. To combine both technologies, 2 degree misorientation is a good compromise and probably will become an industrial standard. In this case, all findings of this work will have to be taken into account.

ACKNOWLEDGEMENT

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MECHANICAL PROPERTIES OF LATERAL EPITAXIAL OVERGROWN GALLIUM NITRIDE

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ABSTRACT

Nanoindentation has been used to investigate and compare mechanical properties of GaN grown by the lateral epitaxial overgrown (LEO) method and its defective seed prepared by metalorganic chemical vapour deposition (MOCVD). Common modulus of elasticity value (~230 GPa) and hardness value (~19 GPa) were found for both materials. The GaN response to nanoindentation was found to be purely elastic for low indentation loads (below ~250μN) with the onset of plasticity being marked by discontinuities or "pop-in" events in the indenter load-penetration curves. The maximum shear stress under the indenter at "pop-in" events for LEO GaN corresponds well with the critical shear stress necessary for homogeneous dislocation nucleation indicating that the defects in this region are too sparse and do not aid in dislocation nucleation.

1. INTRODUCTION

GaN and its related alloys are widely used to fabricate blue light emitting diodes and laser diodes as well as high-power, high-frequency electronic devices [1]. However, due to the lack of lattice-matched substrates conventional heteroepitaxial growth results in large densities of extended defects (~10^9 cm^{-2}) deteriorating the optical and transport properties of GaN-based films [2]. One way to reduce this defect density is to use the lateral epitaxial overgrowth (LEO) method [3], which consists of partially covering a conventional GaN layer with a dielectric mask and performing subsequent regrowth, so that low defect density (~10^5 cm^{-2}) GaN is overgrown over the masked areas (LEO GaN, or "wings") using the GaN grown in the mask opening as seed (seed GaN, or "window").

2. EXPERIMENT

In this study nanoindentation experiments with a Berkovich three sided pyramid indenter have been performed to investigate and compare mechanical properties of LEO ("wings") and defective seed ("window") GaN prepared by metalorganic chemical vapour deposition (MOCVD).

3. RESULTS AND DISCUSSION

It has been found that both "wings" and "window" material shared the same modulus of elasticity value (~230 GPa) and the same hardness value (~19 GPa). The GaN response to nanoindentation was found to be purely elastic for low indentation loads (below ~250μN) with the onset of plasticity being marked by discontinuities or "pop-in" events in the indenter load-penetration curves. The maximum shear stress under the indenter at "pop-in" events for "wings" GaN corresponds well with the critical shear stress necessary for homogeneous dislocation nucleation indicating that the defects in this region are too sparse and do not aid in dislocation nucleation. However, for the "window" GaN the maximum shear stress under the indenter at "pop-in" events was significantly reduced in comparison to LEO GaN suggesting that the onset of plasticity in the "window" GaN is triggered from existing dislocations that assist the nucleation of indentation-induced slip during loading.

4. SUMMARY

Common modulus of elasticity value (~230 GPa) and hardness value (~19 GPa) were found for both LEO GaN and its seed GaN material. The GaN response to nanoindentation was found to be purely elastic for low indentation loads (below ~250μN) with the onset of plasticity being marked by discontinuities or "pop-in" events in the indenter load-penetration curves. The value of the maximum shear stress under the indenter at these "pop-in" events suggests that the onset of plasticity in the defective seed GaN is triggered from existing dislocations, in contrast to LEO GaN where homogeneous dislocation nucleation is indicated

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CARBON-DOPED P-TYPE (0001) PLANE AlGaN (Al=0.06 TO 0.50) WITH HIGH HOLE DENSITY

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ABSTRACT

In this paper, we want to report and to discuss deeply on our recent promising experimental results on the electrical conduction properties of carbon-doped (C-doped) p-type AlGaN that we have succeeded.

P-type conduction was experimentally achieved in the C-doped (0001) plane AlGaN with small amount to about 50% of Al solid composition, but not GaN with no-Al composition. Maximum hole density (determined by the van der Pauw geometry Hall-effect measurement) that we have achieved for the AlGaN layers with Al compositions of 6%, 10%, 27%, and 55%, was in the range of p= (1-3) x 10 ^{18} cm^{-3}. And "maximum effective ionized acceptor density (N_A-N_D)", which was determined by Capacitance-Voltage measurement, was also nearly same value.

1. INTRODUCTION

Electrical conduction control of p-type AlGaN was extremely difficult problems to be solved from the scientific and technical points of view. Magnesium (Mg) was unique p-type dopant for GaN and AlGaN [1-2]. However, it was well known that the acceptor energy level of the Mg was about 230 meV in a GaN (experimental value), and became deeper in an AlGaN than that in a GaN. Therefore, electrical conductivity of the Mg-doped AlGaN was extremely low for optical applications, such as light emitting diode (LED) and laser diode. On the other hand, we can find several papers in which p-type conductivity was demonstrated in the C-doped hexagonal (1-101) and another plane GaN [3-7], or no achievement of p-type conduction in the C-doped GaN [8]. In this paper, we are discussing on the high hole-density (0001) plane AlGaN concluding our recent experimental results.

2. GROWTH PROCEDURE

GaN and AlGaN layers were grown on a (0001) plane sapphire substrate by a conventional Low Pressure Metal Organic Vapor Phase Epitaxy process. Typical growth pressure and growth temperature were 40 mbar and 1180 ℃, respectively. Source materials of Ga, Al, C, and N were TMGa, TMAl, CBr_4, and NH_3, respectively.

Typical sample structure was as follows. Thick n-type GaN or AlGaN (2-4 μm of thick) template was grown on the high temperature un-doped AlN (few nm of thick) and un-doped (AlGaN/GaN) multi-buffer layers, and then, C-doped AlGaN (1-1.5 μm of thick) was grown on the n-type GaN or AlGaN template. Thin Mg-doped GaN cap-layer was grown on the C-doped AlGaN, if the cap layer was necessary for Capacitance-Voltage (C-V) and Hall effect measurements using small Ohmic-contact and anti-oxidation layers.

3. EXPERIMENTAL RESULTS

3-1 Hall effect measurement

Un-doped AlGaN layers were all n-type, and background electron concentration was in the range of n ≈ (3-9) x 10^{15} cm^{-3}. Typical Hall mobility of these samples was in the range of 20-80 cm^2/Vs at room temperature.

Figure 1 is our Hall effect measurement results of C-doped AlGaN with 10 % of Al solid composition at room temperature. Type of electrical conduction and carrier concentration of C-doped AlGaN were n-type and carrier density were in the range of n ≈ 3x10^{14} to ≈ 9x10^{15} cm^{-3} in the small CBr_4 flow rate region of 0.06 to 0.3 μmol/min, respectively. The carrier concentration was decreased, for once, down to n≈5x10^{14} cm^{-3} at 0.7 μmol/min. Then, type of electrical conduction have changed from n-type to p-type above the CBr_4 flow rate

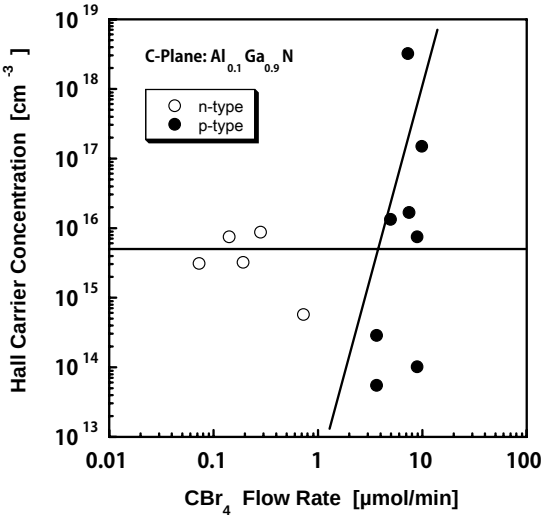


Fig. 1: Dependence of Hall carrier concentration on CBr_4 flow rate for carbon-doped $Al_{0.1}Ga_{0.9}N$ obtained by van der Pauw geometry Hall measurement. Open and closed circles indicate n-type and p-type conductions, respectively.

of about 3 µmol/min and hole concentration increased

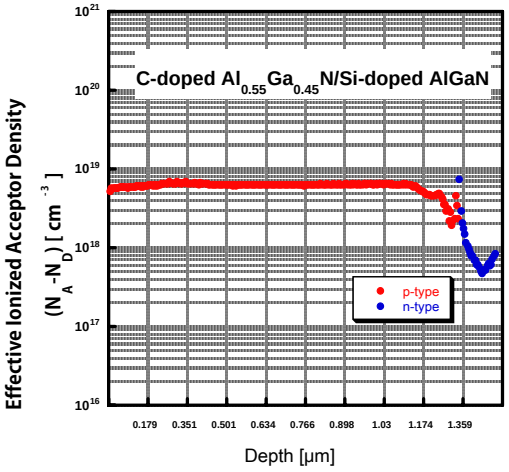


Fig. 2: Depth profile of Effective Ionized Acceptor Density for carbon-doped AlGaN with 55% of Al solid composition.

drastically from p≈4 x 10^{13} cm^{-3} to p ≈ 3x 10^{18} cm^{-3} depending on the CBr_4 flow rate. Hall mobility of the C-doped AlGaN in the p-type region was around 0.9-20 cm^2/Vs (at p ≈ 3x 10^{18} cm^{-3}) at room temperature.

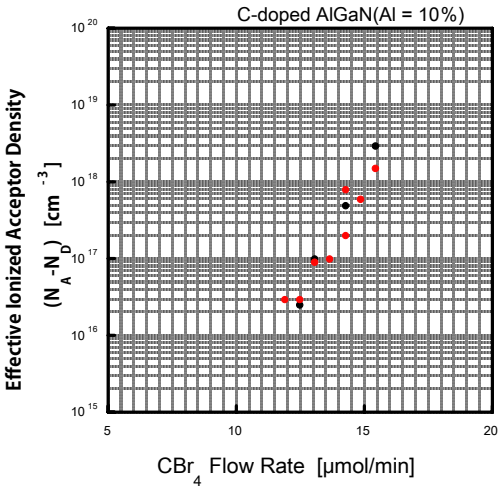
3-2 C-V measurement

C-V measurement was also examined for the C-doped AlGaN in order to determine Effective Ionized Acceptor Density (EIAD=(N_A-N_D) at room temperature, where N_A and N_D are ionize accepter and donor densities, respectively). The C-V measurement can make clear the characteristic of the p-type conduction of the C-doped AlGaN.

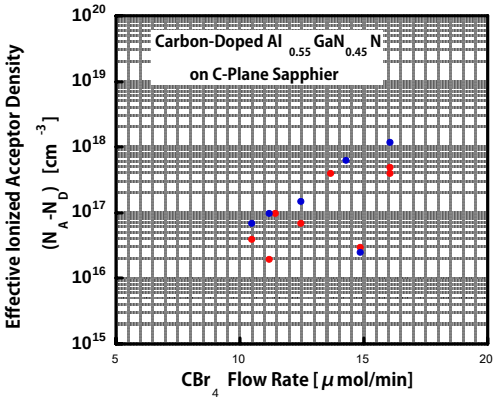
Figure 2 is one of our depth-profile data of the EIAD which was determined by C-V measurement for the sample structure of Mg-doped GaN(0.18 µm thick)/C-doped AlGaN (Al=55%, 1.0 µm thick)/Si-doped AlGaN (Al=0.55, 2-4 µm thick). Electrical conduction type of the C–doped AlGaN with Al=0.55 was p-type and the EIDA was fixed to 6-7x 10^{18} cm^{-3} from 0.18 µm to 1.2 µm of depth (this is completely equal to the layer thickness of C-doped AlGaN). On the other hand, the EIDA of Mg-doped GaN was slightly small and was 5x 10^{18} cm^{-3}.

Figure 3-(a), and –(b) are dependence of the EIDA of the AlGaN with 10% and 55% of Al solid composition. As shown in Fig. 3-(a) and –(b), the EIAD were easily controlled from 3x 10^{16} cm^{-3} to 3x 10^{18} cm^{-3} by changing flow rate of the CBr_4.

In conclusions, we have experimentally achieved high hole density AlGaN layer by carbon-doped AlGaN with small amount to 55% Al solid composition. Maximum hole density that we have achieved was p ≈ 3x 10^{18} cm^{-3}.



(a): Carbon doping characteristic of AlGaN with 10% of Al solid composition



(b): Carbon doping characteristic of AlGaN with 55% of Al solid composition

Fig. 3-(a) and (b): Dependence of EIDA on the CBr_4 flow rate for AlGaN with (a) 10% and (b) 55% of Al solid composition

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CARRIER TRANSPORT IN ANNEALED INHOMOGENEOUS Au/Ni/p-GaN INTERFACES

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ABSTRACT

In this paper, the evolution of the electrical proprieties of Au/Ni bi-layers upon annealing in N_2/O_2 is reported. The specific contact resistance ρ_c improved with increasing annealing temperatures, with an optimal condition obtained after annealing at 600°C. The temperature dependence of ρ_c indicated that thermoionic field emission (TFE) is the dominant transport mechanism at the annealed inhomogeneous Au/Ni/p-GaN interface, and an effective barrier height of 0.71 eV was determined. The results were compared with previous literature assumptions, and a correlation between the electrical data and the interfacial microstructure was proposed.

1. INTRODUCTION

The wide band-gap and the high critical electric field of GaN-based materials make them ideal candidates for high temperature and high-power electronic devices. In this context, it is important to develop good Ohmic contacts with a low specific resistance. While for n-type GaN there are different schemes to achieve low specific contact resistance ρ_c [1], for p-type GaN the formation of good Ohmic contacts is still a challenge, due to the difficulty to increase the carrier concentration of p-type impurity (like Mg), to the high ionization energies of dopants, and to the difficulty to find metals with a low Schottky barrier. Some authors reported on the use of Au/Ni bi-layers as potential route to promote the formation of Ohmic contacts to p-GaN [2,3]**.** In particular, an improvement of the specific contact resistance for a Au/Ni bi-layer could be achieved by annealing in oxidizing ambient. Although different explanations on the Ohmic contact formation were proposed [4,5], the current transport mechanism was not fully discussed yet and the correlation between structural and electrical data remains still controversial. In addition, most of the works have been finalized to optoelectronics applications, proposing very thin (semitransparent) metal layers as Ohmic contacts, that instead may be not a suitable approach for power electronics devices.
In this work, the electrical and structural evolution of Au/Ni contacts to p-GaN upon annealing was monitored. The temperature dependence of ρ_c was modeled, extracting the barrier height. A correlation with the structural properties of the annealed metal layer was proposed.

2. EXPERIMENT

Mg-doped p-type GaN epitaxial samples, 0.5 μm thick, with a net hole carrier concentration of 6.8×10^{17} cm^{-3}, were grown on a (0001) sapphire substrate. A thin heavily doped p-GaN cap layer (with a Mg concentration of 1.5×10^{20} cm^{-3}) was grown to facilitate the Ohmic contact formation. Ni (20nm) and Au (80nm), were sequentially deposited on the sample surface, and patterned by lithography and wet etch, defining transmission line model (TLM) structures for electrical characterization. Then, the samples were subjected to rapid thermal annealing in N_2/O_2 in the range 400-700 °C. The structural characterization was carried out by X-Ray Diffraction (XRD) and Transmission Electron Microscopy (TEM).

3. RESULTS AND DISCUSSION

While the as-deposited Au/Ni bilayer showed a strong rectifying behavior, an improvement of the current–voltage (I-V) characteristics occurred after annealing above 400 °C. Fig. 1 shows the I-V curves measured on TLM patterns at a distance of 5 μm, for different annealing temperatures. Clearly, with increasing annealing temperature an increase of the current (and a trends towards the Ohmic behavior) occurs. The best suited condition was reached at 600 °C, where a specific contact resistance $\rho_c = 2\times10^{-3}$ Ωcm^2 was determined.
The improvement of the I-V characteristics was correlated to the formation of NiO into metal layer. In fact, from the XRD spectra (see Fig. 2), peaks associated to the formation of NiO appear after annealing at 500 °C, and they increase in intensity at higher temperature. Clearly, as also reported by other authors [4], there exists a correlation between the structural evolution of our proposed bi-layers (characterized by the formation of NiO) and the improved electrical characteristics.

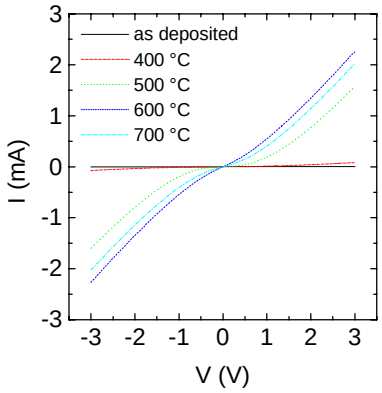

Fig. 1: I-V curves of Au/Ni contacts to p-GaN, annealed in N_2/O_2 at different temperatures.

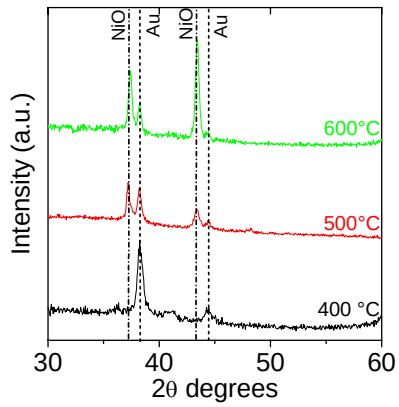

Fig. 2: XRD patterns for Au/Ni contacts to p-GaN, annealed in N_2/O_2 at different temperatures.

TEM analyses in cross section (not reported) showed an inhomogeneous metal/p-GaN interface, characterized by the presence of an almost uniform Au layer interrupted by NiO inclusions around 250 nm wide. Most of the oxidized Ni is observed on the top of the metal contact as a NiO layer with a mean thickness of about 50 nm.

In order to identify the dominant carrier transport mechanism and determine the value of the barrier height, the temperature dependence of ρ_c was studied in the range 25-150 °C. As can be seen in Fig. 3, the values of ρ_c decrease with increasing temperature. Thermoionic field emission (TFE) [1] was the model that better described the experimentally observed trend of ρ_c. The fit of the data allowed to determine a barrier height Φ_B of 0.71 eV and a carrier concentration N_A of 5×10^{19} cm^{-3} (this latter very close to the nominal Mg concentration).

Previous works reported a high specific contact resistance 2.6×10^{-2} Ωcm^2 for a uniform Au/p-GaN contact [6]. Hence, the formation of NiO and its presence at the interface is a key factor to improve the electrical characteristics. Furthermore, the Schottky barrier height values expected for the Au/p-GaN and NiO/p-GaN contact are 1.78 eV [7] and 2.28 eV [8], both higher than the experimentally determined value of 0.71 eV found in our sample. The measured value of 0.71eV can be considered as an effective barrier height of the inhomogeneous system in which Au and NiO coexist at the interface to p-GaN. The low barrier height of this inhomogeneous interface can explain the improvement of the specific contact resistance. However, it cannot be ruled out that the underlying GaN, in the proximity of the interface with the metal, was modified by the out-diffusion of Ga or N atoms during annealing. Further investigation are needed to definitively clarify this issue.

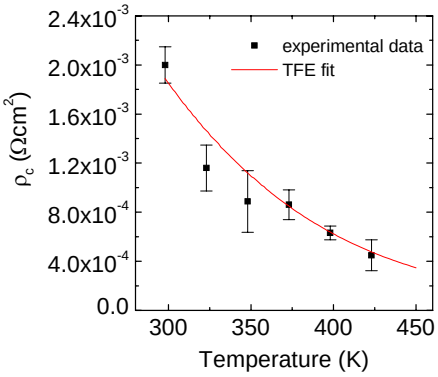

Fig. 3: Specific contact resistance ρ_c as function of temperature.

4. SUMMARY

The structural and electrical evolution upon annealing of Au(80nm)/Ni(20nm) bi-layers for Ohmic contacts to p-GaN was studied. A specific contact resistance of 2×10^{-3} $\Omega\cdot cm^2$ was found at room temperature, and it decreases with increasing temperature following the TFE model. A correlation between electrical and structural measurements established that the formation of NiO play a fundamental role for the Ohmic behavior of the contact. From the fit of the experimental data with the TFE model, a low barrier height value of 0.71 eV for the annealed inhomogeneous Au/Ni/GaN interface, that can be responsible for the improved electrical properties,

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ANALYSIS OF THE LEAKAGE CURRENT OF AlGaN/GaN SCHOTTKY DIODE DEPENDENT ON OHMIC CONTACT PAD ELECTRODE POSITION

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ABSTRACT

Recent progress in a wide band-gap GaN based high electron mobility transistors (HEMTs) has revealed them to be strong candidates for future high power devices at high frequency operation [1]. In order to extract and utilize the favorable GaN material properties, however, there are still a lot of areas to be investigated. Among them the most important is to develop new processes, structure design and characterization techniques. In this paper we present the influence of a reference ohmic metal pad electrode position on the total current through the Schottky diode on the AlGaN/GaN heterostructure. The modified approach of evaluation of the main parameters from the forward *I-V* characteristics is used for the Schottky structure characterisation.

1. INTRODUCTION

Determination of the transport properties and effective Schottky barrier height ϕ_b on GaN and related compound semiconductors with higher precision is important for further analysis of new combinations of metals and semiconductors and better understanding of physical behaviour at the interface. There are many methods of determining of the Schottky barrier height ϕ_b available involving current-voltage (*I-V*) measurements, capacity-voltage (*C-V*) measurements and photoelectron measurements [1-2]. For their simplicity the temperature dependent measurements of the *I-V* characteristics are most popular and commonly used to analyze the transport properties of the Schottky structures. In general, the current transport in the Schottky diode can be described as a contribution of the following mechanisms: thermionic emission (I_{TE}), generation-recombination (I_{GR}), tunnelling (I_{TU}) and leakage (I_{RL}) currents. All of the mentioned current part can be extracted using of the modified model approximation [3-4].

2. EXPERIMENT

The Schottky diodes under investigation were prepared by Ni/Au metallization on a top of the AlGaN/GaN heterostructure (Schottky contact). The reference ohmic contact was created by Ti/Al/Ni/Au metallization (Fig. 1). Two positions of the ohmic contact pad electrode Ti/Au were analyzed. While in a first type structure all pads (expanded contacts) were on the top of the MESA island, the second structure uses pads located down on the GaN buffer layer and the metal layers of expanded contacts go through MESA edge. The second structure configuration is the regular structure used in HEMTs and is frequently used for the gate of FATFET transistors connection.

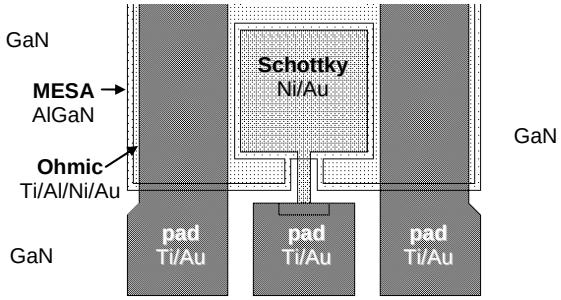

Fig. 1: Layout of the AlGaN/GaN schottky structure.

The measured *I-V* curves of the Schottky diodes at various temperatures are shown in the Fig. 2. The structure with pads located down on the GaN buffer exhibits much higher reverse current. The additional leakage current shows pure ohmic behavior also dominates at low forward biases.

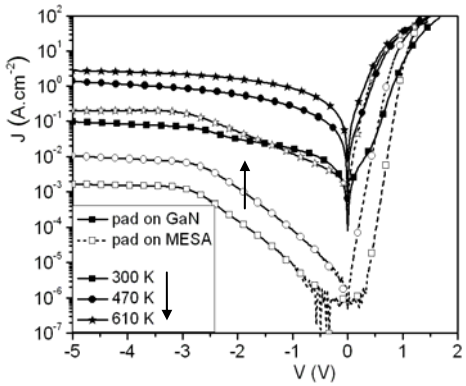

Fig. 2: *I-V* characteristics of the Schottky diodes for different temperatures.

The forward *I-V* part of the Schottky diodes were analysed using of the modified method allows us to assess the effect of particular mechanisms like thermionic emission, generation-recombination, tunnelling and leakage currents [3-4]. The effective Schottky barrier height calculated from the thermionic emission current (Fig. 3b) is about 1.34 eV for both structures. Theirs temperature dependencies exhibit slightly negative

temperature coefficients which correspond to theoretical predictions (Fig. 3a). Comparisons of the Schottky diodes shoved mainly two differences. The structure with pads located down on the GaN buffer exhibits much lower leakage resistance R_L (Fig. 4a). The additional leakage current is caused by direct contact of the ohmic pads allows the current to flow through the GaN layer. The second difference is for the tunnelling current $I_{TU(0)}$ (Fig. 4b). The higher tunnelling current for the structure with pads located down on the GaN buffer should be caused by direct contact of the metal layer and two-dimensional gas (2DEG) located on the MESA edge.

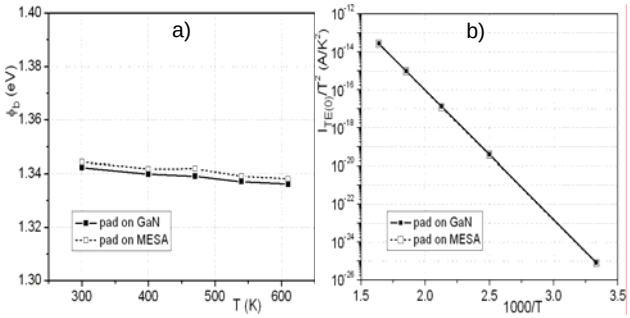

Fig. 3: Temperature dependents of the a) Schottky barrier height ϕ_b and b) thermionic emission current of the diodes.

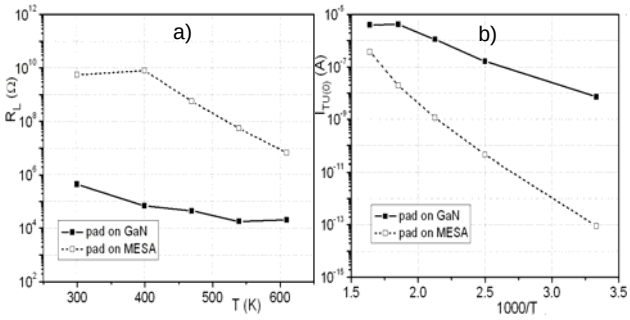

Fig. 4: Temperature dependents of the a) leakage resistance R_L and b) tunnelling current of the diodes.

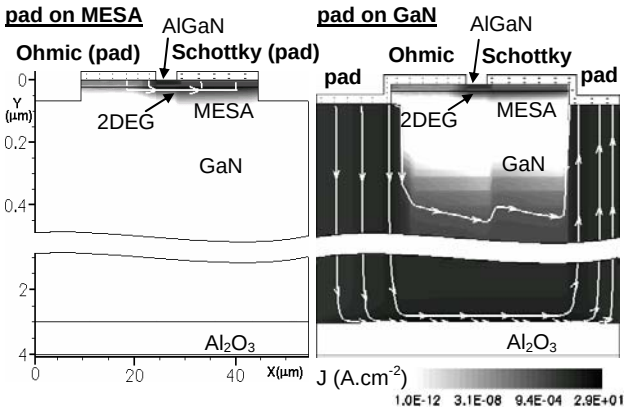

Fig. 5: Current density distribution at V = -3 V for the Schottky diodes.

Two-dimensional electro-physical simulation of the device structures shows and confirms that the additional leakage current is originated by a current path through the GaN buffer layer (Fig. 5). The Schottky current should flow only through 2DEG channel located on the MESA layer. While for the structure with pads located down on the GaN buffer layer the current flows also through the GaN layer. The high resistivity of the GaN buffer layer is decreased with the traps located on the layer. The direct contact of the pads allows the current to flow through the GaN layer. The leakage current is dominant for reverse and low forward biases. The comparisons of the measured and simulated *I-V* curves of the Schottky diodes are in Fig. 6.

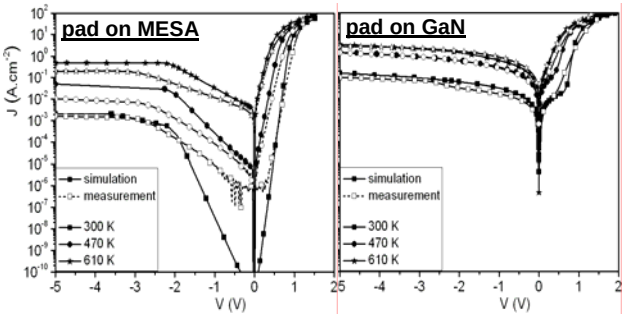

Fig. 6: Comparisons of the measured and simulated *I-V* curves of the Schottky diodes.

3. CONCLUSION

The analysis of the *I-V* curves of the Schottky diodes shows the anomalous behavior of Schottky structure with pads located down on the GaN buffer. An additional mechanism of the leakage current flowing through the contact pad due to traps inside GaN buffer increases the conductivity of the layer. The good quality and high resistivity of the GaN buffer layer under the contact pads is necessary to supress the leakage component of the Schottky gate current flowing in FATFET transistors. The good agreement between the measurements and simulations confirms the validity of our modified approach.

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PROCESS STABILITY STUDY OF MASS PRODUCTION OF LED STRUCTURES BY MOCVD

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In this study we present recent data on the process stability for LED production in the 56x2" and 14x4" configuration of the AIX G5HT. Consecutive run to run (r2r) as well as stability data with changed reactor hardware under the same recipe are presented.

The investigated structure consists of a 5 period InGaN/GaN LED structure with 2.7 nm thick wells, AlGaN electron blocking layer and p-doped GaN cap. All layers were characterized using photoluminescence mapping (PL), high-resolution X-Ray (HRXRD) and white-light interference thickness mapping (WLI).

In the 56x2" configuration 9 batches of runs with 14 wafers each with the exact same recipe were grown. In between the batches intentional hardware changes were made to assess the process stability of the tool. At an average wavelength of 467.1 nm a total wavelength spread of ±1.2 nm was found for all wafers. The wavelength results showed a random behavior without any signs of drift indicating an excellent invariance of the tool and process to changing deposition and hardware conditions in the reactor. The on-wafer wavelength standard deviation was around 0.9 nm without edge exclusion.

To verify the stability of the growth system in the 14x4" configuration 3 consecutive runs with 2 loaded 4 inch wafers each were performed. At an average PL wavelength of 453.4 nm a total spread over all 6 wafers of ±1.5 nm was found. The average wavelength standard deviation on wafer was 0.7 nm.

The XRD-rocking curve full-width-at-half-maximums (FWHM) for the structures were 245.9 arcsec and 250.9 arcsec for the (002) and (102) peak, respectively. HRXRD traces showed well resolved MQW fringes up to the 6th order. The average MQW pair thickness could be determined to 20 nm with a total spread of ±0.5 nm over all wafers.

Further results on HRXRD, process monitoring and thickness measurements will be presented.

InN, AlN, GaN FILMS ON FIANITE SUBSTRATE AND BUFFER LAYER

Yu.N. Buzynin[1*], O.I. Khrykin[1], A.N.Buzynin[2], A.Yu. Lukyanov[1], V.V.Osiko[2], V.G.Shengurov[3], M.N. Drozdov[1], Yu. N. Drozdov[1], B.N.Zvonkov[3], S.A.Denisov[3]

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ABSTRACT

In this work we present the results of investigation on fianite application as monolithic substrate and buffer layers for III-N epitaxy. The InN, AlN and GaN films were grown by the conventional MOCVD including the «capillary epitaxy» technique.

1.INTRODUCTION

Fianites are single crystals of zirconia- or hafnia-based cubic solid solutions with yttrium, calcium, magnesium or lanthanides (from gadolinium to lutetium) stabilizing oxides (ZrO_2 (HfO_2)·R_2O_3, where R - Y, Gd … Lu). The technology of synthesis of the ZrO_2 –based single crystals was for the first time developed in Russia in the Lebedev Physical Institute of the Russian Academy of Sciences (FIAN) [1]. Worldwide these crystals are mostly known as «cubic zirconia» (CZ), or «yttrium stabilized zirconia» (YSZ). Due to a unique combination of physical and chemical properties fianite is extremely perspective multipurpose material for new electronic technologies [2] in particular as a substrate and a buffer layer for Si, Ge and A_3B_5 epitaxy. Use instead of fianite crystals its thin layers on GaAs and Si substrates will allow to remove restrictions on the size of structures and to lower their cost.

2.EXPERIMENT

The InN, GaN, AlN films were grown on fianite (111), (100) substrates without and with Ge, GeSi, GaSb, GaAs: Sb and superlattice InAs/GaSb buffer layers and also Si (111), (100) and GaAs (100) substrates with single(fianite) and double(fianite/poro Si, GaAs) buffer layer by the conventional MOCVD and «capillary epitaxy» techniques [3]. The Ge, GeSi layers were received by a hot wire chemical vapor deposition, GaSb, GaAs: Sb and superlattices InAs/GaSb - by a laser and fianite layers-by magnetron deposition methods. The structural quality and electrophysical and photovoltaic characteristics of the obtained epitaxy films and structures were examined by the standard X-Ray diffractometry, optical and atomic force microscopy, scanning and transmission electron microscopy, secondary ion mass-spectrometry, and photoluminescence.

Conditions of growth of mirror smooth monocrystal Ge, GeSi, GaSb, GaAs:Sb and InAs/GaSb superlattices buffer layers on fianite substrates(SL) are defined. So, the FWHM X-ray rocking curves for these GaSb and SL InAs/GaSb buffer layers on fianite (111) substrates has made 0.23° and 0.24°, accordingly, and a roughness of their surface does not exceed 4 nm. It is shown that this $A^{III}B^{V}$ layers may be used as buffer in the epitaxy of $A^{III}N$. The use of these buffer layers allowed obtaining of continuous uniform GaN films on fianite substrates with orientations (100) and (111) by MOCVD.

GaN films were grown on fianite substrates using three types of nucleating layers:

1. A low-temperature GaN layer annealed in a hydrogen—ammonia atmosphere. The substrate temperature (T_s) - 650°C during growth and 1000°C during annealing.
2. A low-temperature AlN layer annealed in a hydrogen—ammonia atmosphere at 1000°C.
3. A high-temperature AlN layer (T_s - 1100°C).

The fianite substrate was annealed in pure hydrogen at ~1070°C before the deposition of a nucleating layer. In growing epitaxial layers of $A^{III}N$ and other $A^{III}B^{V}$ compounds, hydrogen (which can be purified quite easily) was usually employed as the carrier gas. For $A^{III}N$ epitaxy, however, it was shown that these compounds are unstable in hydrogen and are etched at the growth temperatures, in contrast to other $A^{III}B^{V}$ compounds. The use this nucleation layers on fianite substrates (111) and (100) allowed us to obtain continuous and uniform single-crystal GaN films of hexagonal modification **(**Fig.1).

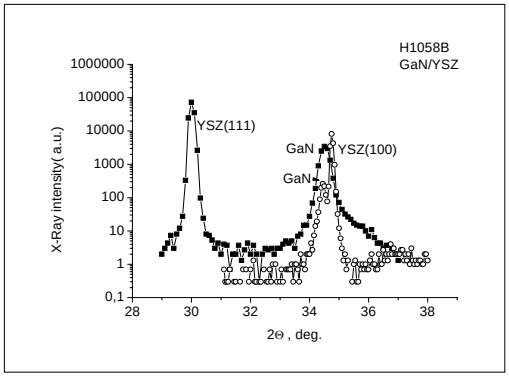

Fig.1: XRD of GaN films on YSZ (111) and YSZ (100)

The layers were smooth and uniform and their surface roughness did not exceed 0.6 nm. A SIMS analysis of an AlN film on cubic zirconia revealed that the layers were

b

uniformly distributed over the width elements, with a very sharp concentration profile of the Zr atoms on heteroboundary (Fig.2.).

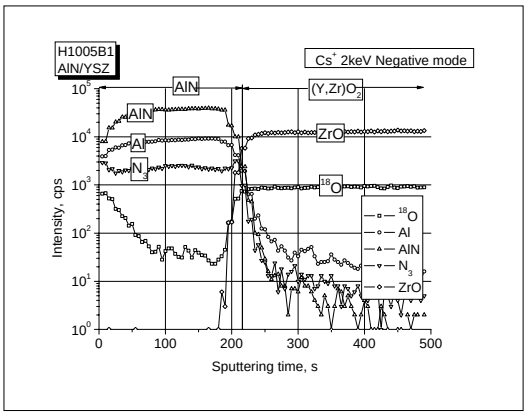

Fig. 2: Results from a layer-by-layer SIMS analysis of AlN film on a fianite substrate

Comparative researches by SEM methods of GaN films on Si and GaAs substrates with single(YSZ) and double(YSZ/por Si) buffer layers have shown, that use of double buffer layers with porous layer more than 10 times reduces concentration and electric activity of defects in GaN film and raises its electric uniformity.

The InN films is commonly grown on (0001) sapphire substrates, incorporating an AlN and/or GaN buffer layer. The lattice mismatch between these buffer layers and the InN film is, however, large 14% and 11%, respectively. This mismatch relaxes largely through the introduction of threading dislocations, and these have been shown to be one source of the high unintentional *n*-type conductivity observed in InN films grown to date [4,5]. Recently, fianite has been investigated as an alternative substrate for growth due to its much smaller lattice mismatch with InN of only 2.5%. Fianite substrates were successfully used to obtain heteroepitaxial InN films by RF-MBE [6,7]. Single-crystal InN films on fianite (100) substrates are received by MOCVD method in our work for the first time. X-Ray rocking curve of InN films grown on Al_2O_3(0001) and fianite (100) substrates were shown at Fig.3.

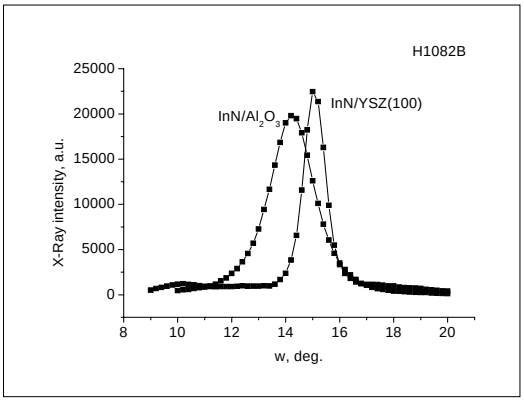

Fig. 3: X-Ray rocking curve of InN films

The InN films 0,3 μm thickness are received in N_2 as carrier gas under the high effective V/III ratio at the temperature interval 550-650°C. Diffraction peaks InN(0002) and In(101) are observed at 2θ=31.3° and 2θ=33.0°, accordingly on the X-ray 2Q/ω scan. The In(101) peak was observed also by authors [7] at growth InN films on fianite by RF-MBE method. For comparison we will tell, that InN films grown by us on sapphire substrates with GaN buffer layer under the same conditions of growth has the full-width at half-maximum (FWHM) of c-InN rocking curve about 0,5°. The photoluminescence spectrum of such film is resulted on Fig.4.

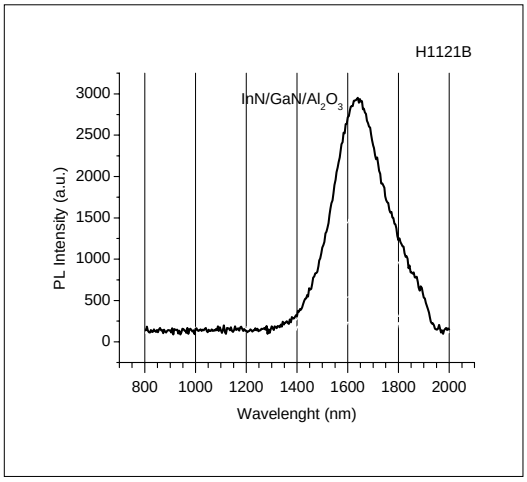

Fig. 4: Photoluminescence spectrum of InN film (300K)

A carrier concentration of $1{,}2\times10^{19}$ cm^{-3} and a Hall mobility of 525 cm^2 /V s are obtained at this InN films.

ACKNOWLEDGEMENTS

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Session 8 :

GaN HEMT devices

Chair : Prof. Elias Muňoz

Tuesday May 31, 11:30 - 13:10

PREPARATION AND PROPERTIES OF GaN-BASED MOSHFETS

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ABSTRACT

Results obtained on AlGaN/GaN and InAlN/GaN MOSHFETs using Al_2O_3 as a gate insulator are reviewed. It is shown that the static as well as high-frequency performances can be improved in comparison to the HFET counterparts. Density of trap states in the MOSHFETs with Al_2O_3 prepared by MOCVD, Al oxidation and ALD techniques are compared. High perspective of GaN-based MOSHFETs with Al_2O_3 gate insulator follows from these results.

1. INTRODUCTION

It is well known that GaN-based heterostructure field-effect transistors (HFETs) are key devices for high-power high-frequency applications [1]. Their mass production has already started [2]. However, performance of HFETs is still influenced by large gate leakage current, DC-RF dispersion and poor reliability of the Schottky contact. Partial suppression of these effects can be obtained by passivation of the material surface. Much better improvement can be obtained by applying a gate insulator on the HFET, i.e. by preparation of a metal-oxide-semiconductor HFET (MOSHFET). First report on AlGaN/GaN MOSHFET with SiO_2 as a gate insulator showed smaller gate leakage current and improved small-signal RF performance comparing to simple HFET counterpart [3]. Investigations of high frequency power performance on similar SiO_2/AlGaN/GaN MOSHFETs have also documented their advantages over HFETs [4,5]. The output power is significantly higher than that of the HFET, as shown in Fig. 1 for measurements at 7 GHz. These results clearly underline an importance and advantages of GaN-based MOSHFETs. Application of various insulators, such as SiO_2, Si_3N_4, Al_2O_3, AlN, ZrO, MgO, HfO, Sc_2O_3, Gd_2O_3 have been investigated [5,6, and references therein]. Nevertheless, many issues related to preparation of GaN-based MOSHFETs are still not solved. Preferable type of insulator and method of its preparation have been not specified yet. Therefore, further extensive studies on these devices are needed.

In this work, results obtained on the AlGaN/GaN and InAlN/GaN MOSHFETs with Al_2O_3 as a gate insulator are presented. The main arguments for choosing Al_2O_3 as a gate insulator are its suitable physical properties [6] and variety of preparation techniques [7]. Properties of the MOSHFETs with Al_2O_3 prepared by metal-organic vapor deposition (MOCVD), oxidation of sputtered Al and atomic layer deposition (ALD) are shown. An improvement of their static as well as high-frequency performance, compared with the HFET counterparts, is demonstrated.

2. EXPERIMENTAL

The AlGaN/GaN and InAlN/GaN layer structures used were typical for HFET application, i.e. about 25-30 nm thick AlGaN (AlN ≅ 25%) or 10-13 nm thick InAlN barrier (InN ≅ 17 %), both grown on GaN buffer (all layers were unintentionally doped) and prepared by MOCVD technique on sapphire, SiC or Si substrates.

2.1. Device processing

Conventional device processing steps known for AlGaN/GaN HFETs were used for the MOSHFET devices. Ohmic contacts were prepared by evaporation of Ti/Al/Ni/Au metal stack and subsequent rapid thermal annealing at 800 °C for 2 min in a N_2/H_2 forming gas atmosphere. Mesa isolation was made by ion beam etching in an Ar plasma. After that an Al_2O_3 layer was deposited between source and drain contacts (details are given in the next section). Finally, Ni/Au gate contacts were patterned by optical lithography or electron-beam lithography (for the gate length ≤1 μm). One- and two-finger MOS-devices with the gate width of 50 μm and 100 μm were prepared. For comparison, HFET counterparts were prepared by the same processing steps as used for the MOSHFETs, however beside Al_2O_3 deposition.

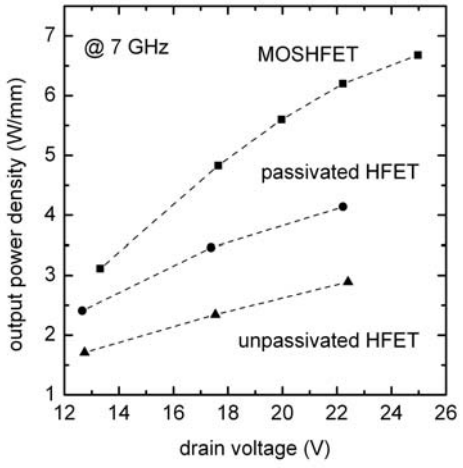

Fig. 1: Output power density of unpassivated and SiO_2 passivated AlGaN/GaN/SiC HFETs and SiO_2/AlGaN/GaN/SiC MOSHFET as a function of drain voltage (f = 7 GHz) [4].

2.2. Preparation of Al_2O_3 gate insulator

The Al_2O_3 gate insulator with thicknesses of 4–14 nm (evaluated by reflectivity or ellipsometry measurements) was prepared by three different deposition techniques:

i) First one is based on low-pressure MOCVD technique and prepared Al_2O_3 gate oxide is designated as MO–Al_2O_3 in the next). Aluminium acetylacetonate dissolved in toluene was used as a metal–organic precursor (Aixtron TriJetTM delivery). Oxygen and argon were used as reaction and transport gases, respectively. The deposition temperature was 600 °C. Devices with the Al_2O_3 thickness ranging between 4 and 14 nm were investigated.

(ii) Sputtering of Al layer and its consecutive oxidation was used to prepare thin Al2O3 gate oxide (designated as Al–ox in the next) as an alternative to above described MOCVD oxides [7]. About 3 nm thick Al layer was sputtered and then oxidized in dry oxygen atmosphere at the pressure of 200 Pa and at room temperature to prepare 4.2 nm thick Al_2O_3 (4SO sample).

iii) Atomic layer deposition technique (ALD) has many advantages, such as low deposition temperature and good thickness controllability [8]. In our case, an Al_2O_3 layer was deposited by ALD technique at 300 °C using trimethylaluminum and water vapor as precursors and N_2 as a carrier gas.

3. RESULTS AND DISCUSSION

The devices were characterized by static (output and transfer) and pulsed *I–V* (0.2–10 μs) measurements, *C–V* and *G–V* measurements at various frequencies (1 kHz – 1 MHz), and small-signal RF measurements (S-parameters).

3.1. Static performance

The output characteristic measurements on MOSHFETs commonly show an increase of the satura-tion drain current compared with the HFET counterparts. An example is shown in Fig. 2 [9]. This effect can be attributed to an increase of the carrier density n_s and/or drift velocity v_d , as $I_{DS}/W_G = q{\cdot}n_s{\cdot}v_d$. An increase of the carrier density due to passivation of surface states is well known [10,11], but it is lower than expected according the drain current increase [12]. On the other hand, an increase of the gate-to-channel separation due to insertion of the oxide layer should result in a decrease of the MOSHFET transconductance compared with the HFET ($g_m = v_d{\cdot}C_{GS}$). However, higher g_m in MOSHFETs than that in HFETs was observed [12]. This indicates on an increase of the effective carrier velocity in the channel [13] because of changed electric field distribution after decreasing the number of surface states in the MOSHFET (virtual gate [14]). In such a way also observed increase of the drain current (Fig. 2) can be explained.

It is well known that high gate leakage current in GaN-based HFETs is a serious problem in general [15].

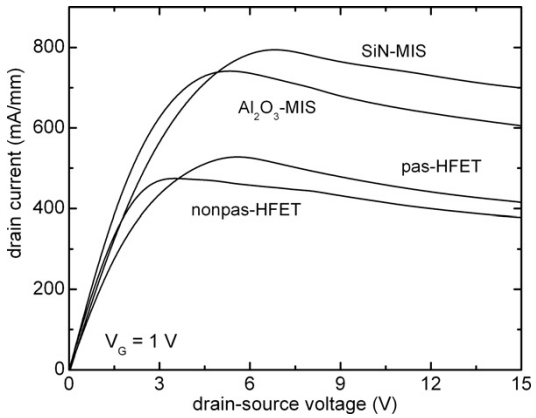

Fig. 2: Output characteristics of Al_2O_3– and SiN– passivated MISHFETs on AlGaN/GaN in comparison with nonpassivated and SiN passivated HFET counterparts [9].

Already first studies on SiO_2/AlGaN/GaN MOSHFETs have shown that the gate leakage current is up to six orders of magnitude smaller than that of the conventional AlGaN/GaN HFETs [3-5]. Similar improvement in the gate leakage can be obtained in InAlN/GaN MOSHFETs, as shown in Fig. 3 [16].

GaN-based transistors are predominantly assigned for high-temperature applications. Therefore performance of AlGaN/GaN HFETs and Al_2O_3/AlGaN/GaN MOSHFETs at elevated temperatures was investigated [17]. The saturation drain current, peak transconductance and the series conductance of the HFETs and MOSHFETs decreased similarly with increased temperature. At 425 °C the devices exhibited ~30% of their I_{DS}, g_m and R_s evaluated at room temperature. All these parameters follow exactly the T^x dependence with a power $x = -1.5$. This indicates that the temperature dependence of the mobility of channel electrons due to phonon scattering is the predominant effect describing high-temperature performance of the AlGaN/GaN HFETs and MOSHFETs.

Temperature dependence of the threshold voltage can be used in order to analyze an influence of traps on performance of HFETs and MOSHFETs. The threshold

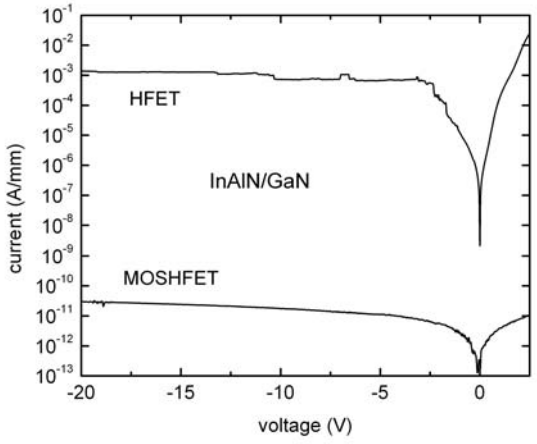

Fig. 3: Two terminal gate-source *I-V* characteristics of InAlN/GaN HFET and Al_2O_3/InAlN/GaN MOSHFET [16].

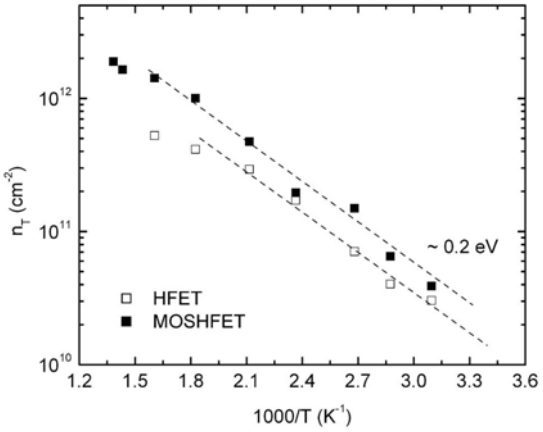

Fig. 4: Trap density as a function of reciprocal temperature evaluated from the threshold voltage shift for AlGaN/GaN HFET and Al_2O_3/AlGaN/GaN MOSHFETs [18].

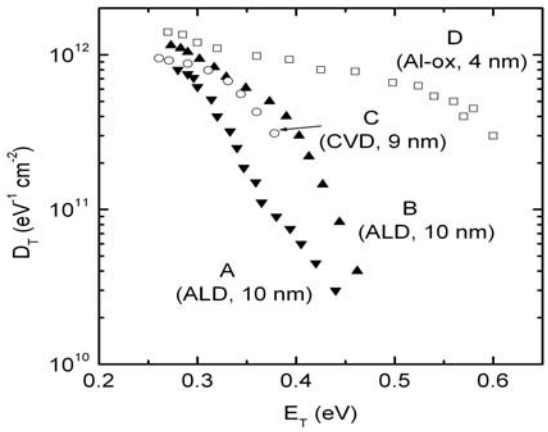

Fig. 5: Trap density as a function of their energy for AlGaN/GaN MOSHFETs with Al_2O_3 gate oxide prepared by different deposition techniques [8].

voltage can be described as $V_{th} = \phi_b - \Delta E_c - (q \cdot n_{tot} \cdot d/\varepsilon_r \cdot \varepsilon_0)$ where $n_{tot} = n_s + n_T$. From measured *V*th one can evaluate the density of trap states n_T, assuming ϕ_b, ΔE_c and the density of shallow carriers n_s to be temperature independent [18]. An example for AlGaN/GaN HFET and Al_2O_3-based MOSHFET is shown in Fig. 4. An identical activation energy of ~0.2 eV can be evaluated for both types of devices. Similar activation energy of 0.21 eV was evaluated from the backgating current measurements and attributed to the buffer traps [19].

3.2. Capacitance and conductance measurements

Material structures used for device preparation can be characterized by channel conductance G_{ch} at low drain voltage (0.1–0.3 V) and *C–V* measurements on large-gate 'fat'-FETs. The drift mobility can be expressed as $\mu_d = (L_G \cdot G_{ch})/(q \cdot W_G \cdot n_s)$, where the sheet carrier density n_s is extracted by the integration of the *C–V* curve. This procedure was applied to AlGaN/GaN device structures [20]. The HFET zero-bias mobility 1630 cm^2/V^{-1} s^{-1} can be well compared with the Hall mobility 1570 cm^2/V^{-1}s^{-1} obtained on van der Pauw patterns. The zero-bias mobility for MOSHFET was 1950 cm^2/V^{-1}s^{-1}, i.e. the mobility enhancement is about 25 %. A higher mobility in MOSHFETs as compared with that in HFETs is attributed to an increase of the effective saturation velocity of the channel electrons [21].

Frequency dependent capacitance and conductance measurements allow to obtain information on the trap states in devices investigated [22]. Parallel conductance can be expressed as $G_p/\omega = (q \cdot D_T/2 \cdot \omega \cdot \tau_T) \cdot \ln[1+(\omega \cdot \tau_T)^2]$, where ω is the radial frequency and the trap time constant $\tau_T = K \cdot \exp(E_T/kT)$. In such a way the density of trap states D_T and their energy E_T can be evaluated from $G-\omega$ measurements and their distribution in the gap follows from data obtained for different gate voltage. An example, D_T as a function of E_T for Al_2O_3/AlGaN/GaN MOSHFETs in which the gate oxide was prepared by three different deposition techniques, is shown in Fig. 5. Remarkable difference in the trap distribution for the CVD, Al-oxidation and ALD techniques indicates an importance of deposition conditions of the gate insulator, particularly its deposition temperature [8]. Additionally it should be noted, that the ALD sample "A" with lowest trap density $D_T \leq 10^{11}$ cm^{-2} eV^{-1} has a 3 nm thick GaN cap layer on top of the AlGaN/GaN heterostructure in contradiction to the other three samples. Different properties of an Al_2O_3/GaN and Al_2O_3/AlGaN interface might be responsible for different trap density evaluated. An improvement in the oxide homogeneity and suppression of fixed charge can be obtained by post-deposition annealing [23]. The range of the trap energy using room temperature analysis is relatively small due limited frequency range commonly used (1 kHz – 1 MHz). Temperature dependent $G-\omega$ measurements can extend the energy range up to about 0.6 eV below the conduction band, as follows from our experiments performed up to 540 K [24].

3.3. High-frequency performance

Small signal characterization of the devices investigated was carried out by on-wafer *S*-parameter measurements. An extrinsic current-gain cut-off frequency (f_T) and a maximum frequency of oscillation (f_{max}) were found from current gain $|h_{21}|^2$ and unilateral power gain GU as a function of frequency. A remarkable increase of the f_T and f_{max} values was found for Al_2O_3/AlGaN/GaN/Si MOSHFETs compared to the HFET counterparts. The peak f_T and increased from 3.2 GHz for the HFETs to 9.6 GHz for the MOSHFETs (2 μm gate length) [9]. Consequently, the peak f_{max} increased from 12.3GHz for the HFETs to 20.4GHz for the MOSHFETs. This confirms the data obtained for the dc transconductances [12,13,21], i.e. the reduction of the MISHFET transconductances is smaller than the gate capacitance decrease. Thus, the cut-off frequency of the MISHFET will be higher than that of the HFET, as $f_T = g_m/2\pi C_G$.

Similar improvement in high-frequency performance can be observed for the Al_2O_3/InAlN/GaN devices, as reported recently [16]. For the HFET, extracted f_T and

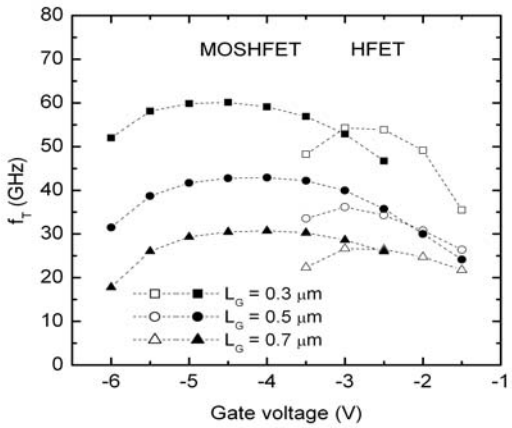

Fig. 6: Current-gain cutoff frequency as a function of gate voltage for Al_2O_3/InAlN/GaN MOSHFETs and InAlN/GaN HFETs with different gate length [16].

f_{max} values were 54 and 58 GHz, respectively (0.3 μm gate length). An increase of f_T to 61 GHz and of f_{max} to 70 GHz was obtained for the MOSHFET devices. The current gain cutoff frequency as a function of gate voltage for the HFETs and MOSHFETs with different gate length is shown in Fig. 6 [16]. These data demonstrate that an enhancement of the MOSHFET RF parameters compared to the HFET ones occurs in all devices investigated. All these indicates that high-frequency performance of GaN-based HFETs can be improved by preparation of MOSHFETs with Al_2O_3 as a gate insulator.

4. CONCLUSIONS

Results obtained on AlGaN/GaN and InAlN/GaN MOSHFETs using Al_2O_3 as a gate insulator were reviewed. It was shown that the static as well as high-frequency performances of both material type devices can be improved in comparison with the HFET counterparts. Density of trap states in the MOSHFETs with Al_2O_3 prepared by MOCVD, Al oxidation and ALD techniques were compared. All these shows high perspective of GaN-based MOSHFETs with Al_2O_3 gate insulator for preparation of reliable high-power and high-frequency devices.

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INFLUENCE OF PASSIVATION ON THE GATE LEAKAGE CURRENT BEHAVIOR OF AlGaN/GaN HIGH ELECTRON MOBILITY TRANSISTORS

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ABSTRACT

In this study AlGaN/GaN High Electron Mobility Transistor (HEMT) devices were investigated regarding their gate leakage behavior in conjunction with the presence of Silicon Nitride (Si_xN_y) passivation. Passivated devices were compared with un-passivated devices, re-passivated devices and devices with an un-passivated region next to the gate in the direction of the drain. Un-passivated devices exhibit very low leakage current while passivation increased the leakage level by several orders of magnitude. Partial reopening of the passivation next to the gate resulted in a drain leakage current reduction to the level of the un-passivated devices; repassivation of the openings re-established the leakage level of passivated devices. This investigation shows clearly that passivation plays a crucial role in controlling the gate-leakage currents in AlGaN/GaN devices.

1. INTRODUCTION

Passivation, usually Si_xN_y in AlGaN/GaN technologies, plays a crucial role in the performance of AlGaN/GaN devices since it reduces current collapse [1] and microwave power degradation [2]. Unfortunately, passivation has been found to significantly increase gate leakage current [3] which can be detrimental to the reliability of devices, since leakage above a certain threshold results in strong device degradation or sudden catastrophic device failure.

Many investigations to date only report the leakage behavior and the paths and mechanisms of the leakage current either of un-passivated or passivated devices [3]-[5], but do not make comparisons in leakage current for devices where passivation is deposited, stripped and subsequently re-deposited during processing.

In this work the leakage current behavior was monitored on wafers throughout the fabrication process. Through the use of specialized test structures it was possible to characterize un-passivated devices, passivated devices, devices with a non-passivated region next to the gate and repassivated devices and to compare the leakage behavior of the devices at the different process steps.

2. EXPERIMENTAL

For this investigation a UMS AlGaN/GaN MMIC technology with L_g=250 nm has been used. Here, dedicated in-line-electrical test modules (process control modules (PCMs)) were developed to realize structures where the removal and re-deposition of SiN layers takes place during the standard process flow. As such, it was possible to gain an insight into the evolution of gate-leakage current due to passivation during processing, without introducing additional processing steps.

Since UMS uses a nitride assisted gate process, it was necessary to enlarge the gate foot opening from 250 nm to 2.5 µm on the modified test structures to generate rectangular rather than T-shaped gates. This was undertaken in order to ensure removal of all SiN residues which might remain at the gate-edge after stripping due to a T-gate profile.

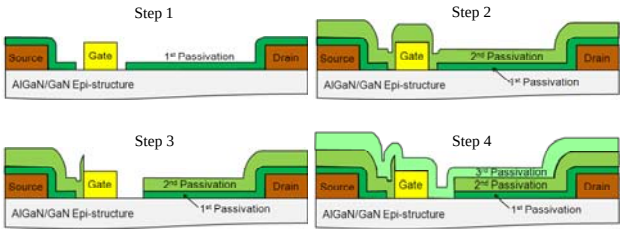

Fig. 1: Condition of the device at the different characterization steps

With reference to Fig. 1, after the gate metal deposition (step 1) the devices were characterized using a Keithley 4200 semiconductor characterization system. A 3-terminal DC-measurement was performed and the leakage current was extracted at V_{gs}= -10V and V_{ds}=10V. Then, the devices were passivated (step 2) and the leakage current measurement was repeated. Nitride free regions next to the gate in the direction of the drain with sizes from 250 nm to 1 µm in 250 nm steps were obtained by dry etching (step 3) – this being achieved through utilization of an etching step within the standard process flow. This was followed by the third characterization using the same measurement conditions as those utilized at steps 1 and 2. The final step was to repassivate the whole structure (step 4) again using a step from the standard process flow and re-measurement for a final time.

3. RESULTS AND DISCUSSION

The 3-terminal characterization of the un-passivated device and the device after passivation are shown in Fig. 2 with the associated SEM pictures of the structures. The extracted leakage current at V_{gs}= -10V for the un-

passivated structure has the very low value of $1x10^{-8}$ A which is equal to 25 nA/mm of gate development.

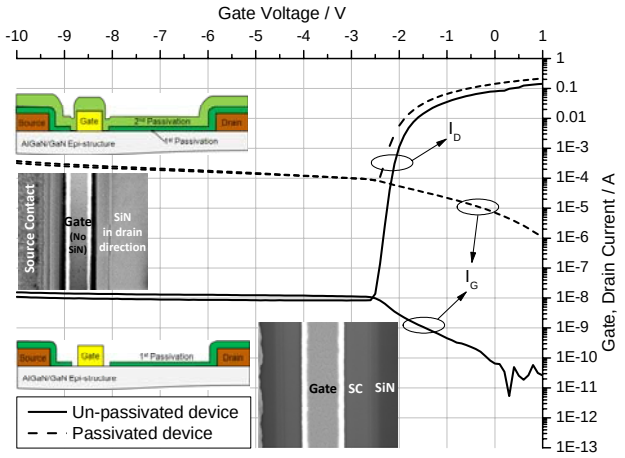

Fig. 2: 3-terminal measurement of the un-passivated and the passivated device

After passivating the device, the leakage current at V_{gs}= -10V increases by more than 4 orders of magnitude to $3x10^{-4}$ A (0.75 mA/mm of gate development), which is a value comparable to that obtained on standard devices using this Si_xN_y passivation type.

In Fig. 3 the 3-terminal characterization of two devices where 500 nm and 1 µm wide areas of Si_xN_y along the complete gate-edge towards the drain have been stripped are shown.

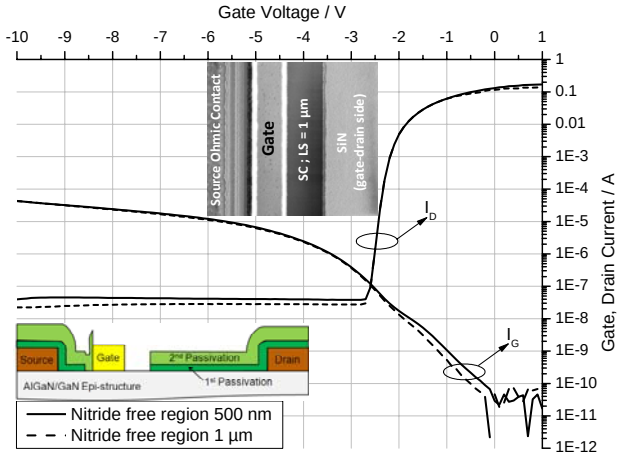

Fig. 3: 3-terminal measurement of two devices where the nitride next to the gate has been removed. The nitride free regions were 500 nm and 1 µm.

Here an interesting observation was made. In this case, the net gate leakage is dominated by the fully passivated Gate-Source diode and remains at a leakage level comparable to the fully passivated device at step 2. However, devices where the nitride has been removed along the gate-edge on the drain side show a large reduction in drain leakage level due to Gate-Drain Diode, which is now partly unpassivated. Here, the value of the leakage current is comparable to the un-passivated device at step 1. The devices with 250 nm and 750 nm nitride free regions showed the same behavior. Based on this observation it can be the stated that the dominant leakage path in the examined UMS devices lies between the semiconductor and the first nitride at the gate edge. If this leakage path is interrupted, by etching away only small amounts of nitride (250 nm) next to the gate, the leakage current drops to a significantly low level. Therefore it is concluded that for the utilized process flow, the leakage current across the semiconductor–metal (Schottky) interface does not play a significant role in the gate-leakage current of passivated devices.

The final 3-terminal characterization after the device is fully repassivated is shown in Fig. 4. It is obvious that the curve of the fully passivated device and the repassivated device are similar, demonstrating that the drain leakage current in the repassivated device is comparable to the fully passivated standard device. This is due to the repassivation of the Gate-Drain diode.

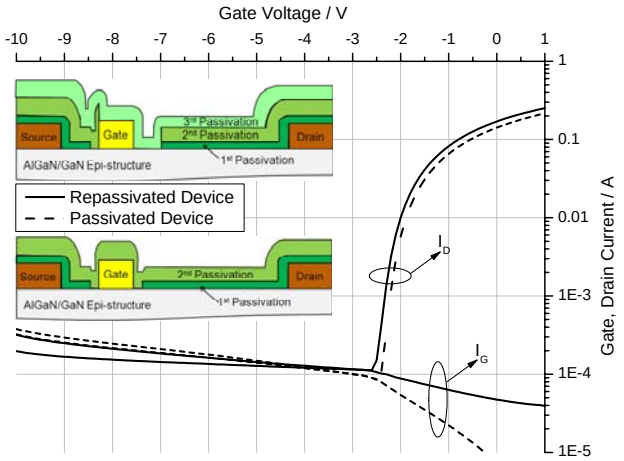

Fig. 4: Repassivated device in comparison with the fully passivated device

4. CONCLUSION

In this investigation un-passivated, passivated, repassivated and partly un-passivated devices have been compared regarding their gate leakage current behavior.

Un-passivated devices showed a very low gate leakage current, while passivation is responsible for an increase in leakage current by more than 4 orders of magnitude. Based on the partly un-passivated structure it was shown that the leakage current path lies between the interface of semiconductor and first nitride at the gate edge. This led to the conclusion that leakage across the Schottky interface is negligible in the case of the measured devices.

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INFLUENCE OF OXYGEN ADDITION IN SiN DRY ETCH PROCESS ON DEVICE CHARACTERISTICS OF PASSIVATED AlGaN/GaN HFETS

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ABSTRACT

In this paper, we report on the impact of processing details on passivated AlGaN/GaN heterostructure field effect transistors (HFETs). The samples were passivated before gate metal deposition, thus gate trenches in the passivation layer had to be opened. Fluorine-based inductively coupled plasma reactive ion etch (ICP-RIE) processes were applied for both samples. The impact of fluorine plasma on the nitrides is well documented. We show that the addition of oxygen influences basic material parameters, DC results and also the RF power performance.

1. INTRODUCTION

For improved DC and RF characteristics, a SiN passivation step is commonly used in AlGaN/GaN HFET processing. This process step can be performed before or after the gate processing. An early passivation before gate processing has some advantages such as a resulting different gate shape. Thereby, the electric field can be modulated, yielding improved device behaviour with respect to current slump.

To open the gate trench, fluorine-based etch chemistries are commonly used. Also the addition of oxygen has been reported [1]. It is motivated by an improved removal of organic residues, which could form non-volatile fluorinated reaction products. Nonetheless, the effect of oxygen addition regarding device performance has drawn little attention so far. In this work we will show the difference between an etch process with oxygen addition and one without. The processes are applied to AlGaN/GaN test structures as well as AlGaN/GaN HFET devices.

2. EXPERIMENTAL

The experiments were performed on material grown by MOCVD. The 4" Si(111) wafer has a ~1.8 µm thick GaN/transition layer stack, an $Al_{0.26}Ga_{0.74}N$ barrier layer of 17.5 nm thickness and a GaN cap of 2 nm.

First, the influence of the etch chemistries on the two dimensional electron gas (2DEG) properties of unpassivated 5 x 5 mm AlGaN/GaN samples was investigated. Using a shadow mask, ohmic contacts (Ti/Al/Ni/Au) were deposited at the edges of the samples by electron beam (e-beam) evaporation, followed by a rapid thermal annealing step at 825 °C for 30 s. The samples were treated in an ICP-RIE chamber with either CF_4/O_2 or CF_4 with gas flow rates of 20/2 sccm and 20 sccm, respectively. The samples were characterised by van-der-Pauw and Hall-effect measurements. Additionally, annealing at 400 °C in a rapid thermal annealer (RTA) for different times was carried out and results were compared with those before annealing.

Based on the above achieved results, two SiN etch processes were selected for the processing of HFETs (A and B). Device isolation was performed by a BCl_3/Ar dry etch process. Ohmic contacts were deposited as described before. The resulting contact resistance was 0.55 Ωmm. Thereafter, 110 nm SiN was deposited by plasma enhanced chemical vapour deposition (PECVD). Subsequently, gate trenches were etched into the SiN with an ICP-RIE process. Sample A was etched completely with CF_4/O_2. To ensure the removal of initial organic residues also for sample B, CF_4/O_2 was used for the first part of the recess process. For the last 20 nm pure CF_4 was employed. The process parameters were adjusted to achieve a sidewall angle in the SiN of 60°. Subsequently, gate contacts (Ni/Au) were deposited by e-beam evaporation. The resulting gate length was 1.30 µm, while the gate width was 100 µm. The gate-drain and gate-source spacing was 2.35 µm and 1.35 µm, respectively. To compare annealing effects with the prepared 5 x 5 mm samples both samples A and B were annealed at 400 °C for 3 min. The samples were characterised before and after annealing with van-der-Pauw and Hall-effect measurements, DC measurements as well as load-pull measurements.

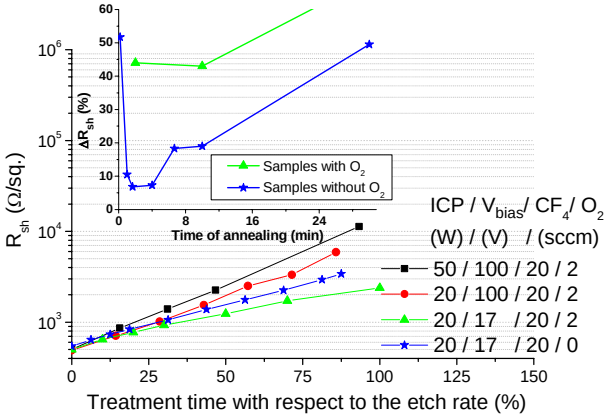

Fig. 1: R_{sh} over time for different etch processes, x-axis is normalised with respect to the etch rate; the inset shows the influence of an annealing step

3. RESULTS AND DISCUSSION

3.1. AlGaN/GaN van-der-Pauw samples (5 x 5 mm)

In fig. 1 the results of CF_4/O_2 and CF_4 treated 5 x 5 mm samples are shown. Although the samples were not covered with SiN, the x-axis is normalised to the corresponding SiN etch depth of each process, while the y-axis shows R_{sh}. As expected, a systematic increase in sheet resistance is observed with longer plasma processing time, but also clearly dependent on the other process parameters. A reduction in ICP power (circles) leads to a reduced increase in R_{sh} as compared to higher power processes (squares), most likely due to a decreased plasma density and therefore with smaller amount of fluorine which can be incorporated into the AlGaN barrier. Decreased ion energy (or bias voltage V_{bias}) also leads to a reduced slope (triangle), which might indicate a reduction in physical damage by ion bombardment. Thus the expected sheet resistance for the same corresponding etch depth is smaller. Also the addition of oxygen leads to a reduced slope (see triangle vs. star). This trend indicates that the oxygen addition inhibits the incorporation of fluorine ions in the barrier.

Furthermore annealing steps at 400 °C under N_2 atmosphere were applied to the samples. In the inset of fig. 1, the difference in R_{sh} between post-anneal state and pre-etch state is shown for different annealing times. For the oxygen-free process (star) R_{sh} can be recovered almost completely for annealing times between 3 and 4 minutes. For the oxygen-containing process (triangle), R_{sh} cannot be recovered, yet it worsens for long annealing times.

Analogues to [2] two effects can be observed: one short-term effect and one long-term effect. The short-term effect is responsible for the recovery of R_{sh}, while the long-term effect is responsible for a degradation effect comparable to the oxygen-containing sample. Thus it cannot be concluded satisfactorily if the main cause of the long-term degradation is fluorine-based or oxygen-based. Nonetheless, it seems that oxygen prevents the observed short-term recovery effect.

3.2. AlGaN/GaN HFETs

From transfer characteristics of the HFETs the saturation drain current $I_{d,sat}$ is extracted to be 600 mA/mm for the oxygen-containing sample (sample A), whereas it is extracted to be 520 mA/mm for the oxygen-free sample (sample B). This confirms the stronger degradation of R_{sh} for the oxygen-free samples as observed already for the 5 x 5 mm samples. Correspondingly, $|V_{th}|$ is higher for sample A. Capacitance measurements at zero Volt proved for both samples that the SiN was etched completely under the gate foot. Thus the difference in V_{th} has to be caused by the different etch chemistry. For both samples gate leakage current is in the order of 0.01 mA/mm @ V_g = - 8 V.

After annealing both samples at 400 °C for 3 minutes, $I_{d,sat}$ of sample A decreases around 7%, while for sample B it is just 2%. V_{th} shifts by 0.1 V to the positive for sample A, while no change occurs for sample B. The annealing results of sample B are contradictory to results shown in the previous paragraph for the blanket etched samples. It is assumed that the metal stack on top of the semiconductor suppresses the expected recovery of R_{sh}. It appears that annealing should be performed before gate metal evaporation.

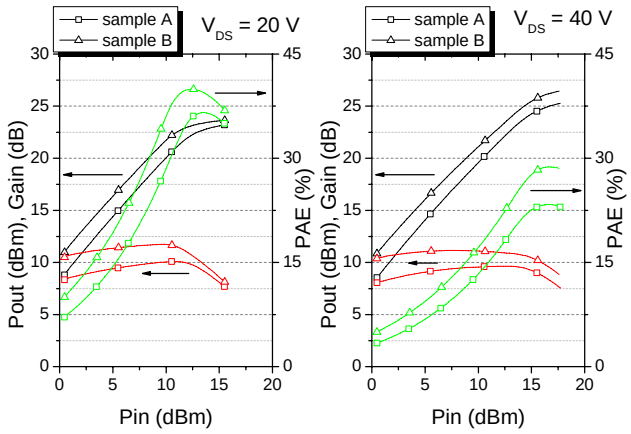

Fig. 2: Load-pull measurements for V_{ds} = 20 V (left side) and V_{ds} = 40 V (right side) at I_{dq} = 7 mA/mm for a 2 x 50 µm x 1.3 µm transistor

RF-power measurements were performed at 2 GHz. The results are shown in fig. 2. The gate quiescent point was chosen to be $I_{d,q}$ = 7 mA/mm. The left graph shows the result for V_{ds} = 20 V, the right one for V_{ds} = 40 V. For V_{ds} = 20 V, saturation power P_{sat} is 2 W/mm and 2.3 W/mm for the oxygen-containing sample and for the oxygen-free sample, respectively. The peak values of the PAE are as high as 36.5% and 40% for sample A and B, respectively. The gain for both samples is around 10 dB, yet there is an obvious difference between both samples, showing a higher gain for sample B.

For V_{ds} = 40 V, the gap between both samples increases. Here P_{sat} is 3.4 W/mm and 4.5 W/mm, while the peak values of the PAE are 23.5% and 29% for samples A and B, respectively. Measurements on larger devices (2x300 µm) confirm this trend.

The apparently contradictory results indicate that oxygen addition to the plasma may mitigate the increase in sheet resistance (loss of sheet carrier density) by fluorine ions, however leads to systematic degradation of the RF performance. Therefore a very balanced adjustment of process parameters is required in order to achieve an optimised result.

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DEPENDENCE OF STATIC AND DYNAMIC GaN HEMT CHARACTERISTICS FROM Fe-DOPED GaN BUFFER PARAMETERS

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ABSTRACT

The influence of Fe-doped buffer parameters on the static and dynamic characteristics of GaN HEMTs have been analyzed by means of two-dimensional numerical simulations. Results obtained on the static characteristics of the simulated devices have shown that thick and highly doped buffers yield better performances in terms of device output conductance and subthreshold conduction, while leaving mainly unaffected other DC parameters. On the other hand, when dynamic characteristics are evaluated, a significant current collapse has been observed pointing out the importance of the correct design of Fe-doped buffer parameters in order to obtain state-of-the-art GaN HEMT performances.

1. INTRODUCTION

GaN HEMTs are currently the most promising power device for the fulfillment of the requirements of modern communication and defense high frequency application. One of the key factor in order to successfully achieve a state-of-the-art GaN HEMTs is the formation of a semi-insulating buffer layer in order to prevent electron current from flowing in the buffer layer and thus grant good pinch off characteristics as well as low output conductance. Aim of this paper is to investigate by means of numerical simulations the dependence of static and dynamic characteristics of GaN HEMTs from the parameters of an iron doped GaN buffer layer.

2. SIMULATED DEVICE STRUCTURE

The device structure used for numerical simulations is depicted in figure 1. Basically, it represent a single heterojunction AlGaN/GaN HEMTs with a 1.8um Fe-doped buffer/channel layer and a 22nm AlGaN barrier layer with a 25% Al-concentration. Iron doping of the GaN buffer layer has been simulated by introducing a depp acceptor level located at 2.5eV from the GaN valence band [1] and by taking into account the exponential decay which is experimentally observed

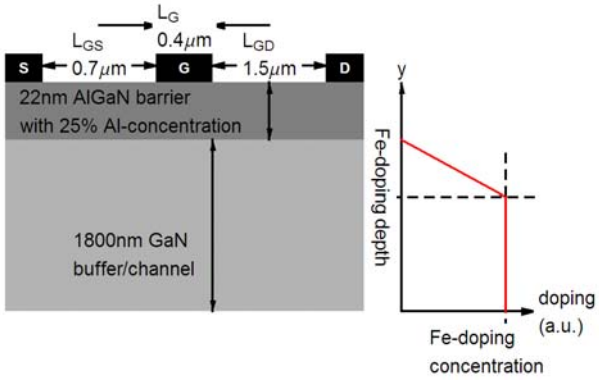

Fig. 1: Simulated device cross-section and iron doping profile used for evaluating the static and dynamic performances.

during the growth of Fe-doped GaN buffers [2]. Particularly, the simulated Fe-doping is taken into account by means of two parameters, see figure 1. The first one corresponds to the Fe-doping depth which corresponds to the thickness of the uniformly Fe-doped region, while Fe-doping concentration corresponds to the dopant concentration during the buffer growth. The experimentally observed exponential decay [2] has been taken into account by reducing the Fe-doping concentration with a rate of 280nm/decade starting from the point where the Fe-doping stops until the AlGaN/GaN heterojunction. Simulations have thus been carried out by varying the Fe-doping concentration from $5x10^{16}cm^{-3}$ to $2x10^{17}cm^{-3}$, and Fe-doping depth from 800nm to 1300nm.

3. STATIC CHARACTERISTICS

The simulated static I-V charachteristics for a 1200nm thick and 1017cm-3 Fe-doped buffer and for a 1300nm thick and 2x1017cm-3 Fe-doped buffer are depicted in figure 2. Generally, it has been observed that thick doped buffers with high concentration resulted in I-V characteristics with good pinch-off characteristics and reduced output conductance. Particularly, the sub-threshold slope at a drain-source voltage of 10V resulted to be very high when using thin buffers, see figure 3. On the other hand, using thick buffers (1200nm-1300nm) improves the sub-threshold behaviour, see figure 3.

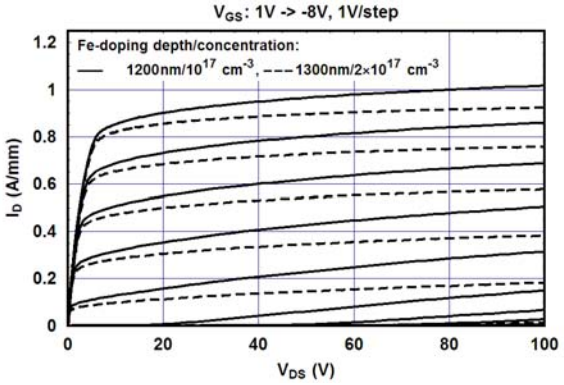

Fig. 2: Simulated static I-V characteristics for two different buffer parameters sets.

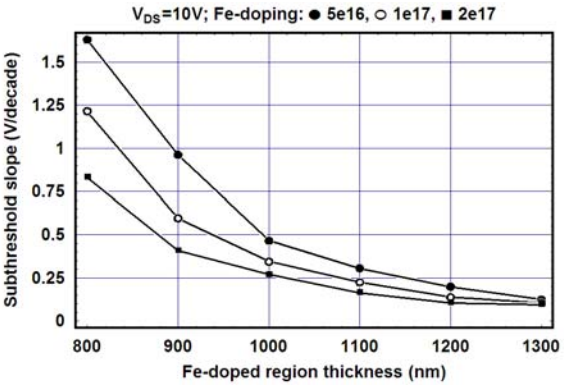

Fig. 3: Extracted sub-threshold slope for several buffer parameters sets at V_{DS}=10V.

Similarly to what observed in terms of sub-threshold characteristics device output conductance has been observed to decrease when using thick and/or highly doped buffers, not shown. On the other hand, the trasconductance peak at V_{DS}=10V was not significantly affected from changing the buffer parameters while the saturation drain current slightly decreased at the increase of the doped buffer thickness and/or doping. Summarizing the results obtained from the static simulations we can thus conclude that for the device studied buffers parameters that allows reasonable DC characteristics are a buffer thickness in the 1200-1300nm range with the high doping leves used in this study, i.e. 1 and $2x10^{17}cm^{-3}$.

4. DYNAMIC CHARACTERISTICS

Based on the results obtained in the previous section, we have also performed transient simulations in order to evaluate the dynamic characteristics of the device simulated. Particularly, a 200ns double-pulse measurement technique has been simulated by pulsing the device from a baseline of V_{GS}=-8V and several V_{DS} values, i.e. pinch-off conditions at high drain voltages. As can be seen in figure 4, where solid lines represent the static I-V characteristics while the closed symbols represent the measured points with the double-pulse measurement technique, a significant current-collapse can be observed for low V_{DS} values. This effect can be

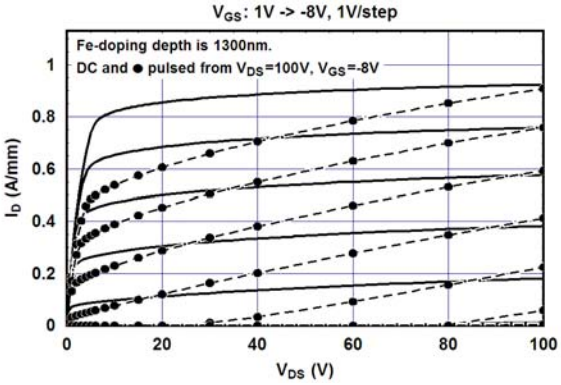

Fig. 4: Comparison between static and dynamic (double-pulse) characteristics for a 1300nm thick and $2x10^{17}cm^{-3}$ doped buffer layer.

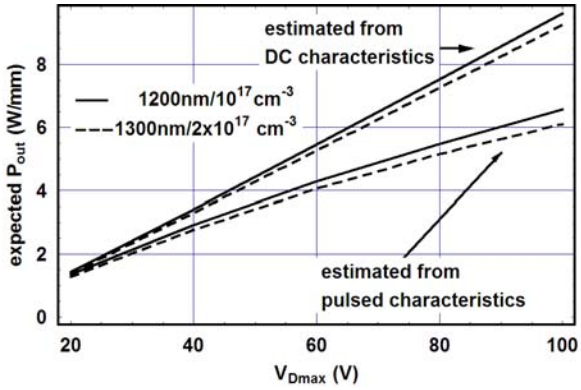

Fig. 5: Estimated output power from DC and pulsed I-V characteristics.

explained by means of electron trapped during the bias at high V_{DS} values in pinch-off conditions [3]. When the device is turned on and V_{DS} is decreased, the trapped electrons do not respond instantaneously thus causing a decrease in the 2DEG concentration of the device. We also estimated the expected output power from the DC and pulsed I-V characteristics assuming to operate the devices at different maximum drain voltages, thus data for the estimation from pulsed I-V have been obtained by extracting I-V characteristics from different drain voltage baselines but with the device always pinched off at V_{GS}=-8V. As can be seen in figure 5 at the increasing of the maximum drain voltage the discrepancy between the expected output power from DC and pulsed I-V increases showing how trapping phenomena in the Fe-doped buffer can significantly affect device operation at high drain voltages.

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SCALABLE GATE TWO EBL STEPS FABRICATION PROCESS FOR OPTIMAL HIGH FREQUENCY GaN HEMT PERFORMANCES

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ABSTRACT

An innovative GaN HEMT technology with scalable L_G down to 80nm, based on a two steps Electron Beam Lithography (EBL) process will be presented. This ensures a low current leakage of the Gate junction and a limited parasitic capacitance associated with a low resistance Gate head. Preliminary results include a very good noise figure (NF_{min}=0.8dB @15GHz), as well as remarkable power performances (P_{OUT}^{Sat}=7.4W/mm).

1. INTRODUCTION

The achievement of record performance in the higher microwave spectra from AlGaN/GaN high-electron mobility transistors (GaN HEMTs) in terms of output power and low noise, combined with high power input signal robustness, is mainly limited to the difficulty to attain a sufficiently high RF gain by L_G downsizing, and simultaneously controlling the associated increase of the detrimental consequences (e.g. short channel effects, Gate current leakage and Drain current slump), enhanced by the application of the high Drain bias V_{DS} required to attain optimum performance [1,2]. A typical solution for many of these issues is represented by the adoption of a Field Plate metal electrode (FP), placed on top of a passivation layer deposited on the semiconductor surface, in order to modulate the electric field (and thus decrease its peak)[3]. This can be achieved either by providing to the Gate metal section an appropriate shape, (e.g. "T"- or "Γ"-like with the head overhanging toward the Drain side of the Gate for a L_{FP} length [4]), but the FP presence also negatively affects the HEMT bandwidth and/or the high frequency RF gain. In fact a suitable FP shape is demanded for best performances, since the increase in L_{FP} contributes to the electric field peak reduction as well as to the increase of the Gate head section area (and thus to the metal wire parasitic resistance R_{GG} reduction). At the same time it contributes to the increase of the Gate parasitic capacitance, most often to the detriment of the RF gain [4,5].
In this work the results achieved from GaN HEMT devices fabricated with an innovative solution (Patent Pending), based on a double EBL process with scalable Gate length L_G and fixed wire resistance, are illustrated. Such process allows a length control down to L_G=80nm, and mitigates the reverse bias Gate current leakage through a post Gate foot metallization annealing thermal process, without introducing any negative effect on the Gate head metallization resistance. The Gate metallization "T"-shape, overlapping beneath Gate foot metallization and the surrounding passivation layer, limits the L_{FP} length and the associated additional capacitance, associated with a large Gate head section area. The fabrication process and the achieved DC, RF, noise and RF power performances are described.

2. DEVICES FABRICATION AND DC CHARACTERIZATION

HEMT's manufacturing has been achieved from an AlGaN/GaN epitaxy on a SiC substrate material, by using a mask set for discrete coplanar waveguide topology discrete devices fabrication with various layout topologies and Gate peripheries W_G. The fabrication process starts with ohmic contact formation for drain and source electrodes definition; then, active device isolation is obtained by using ion implantation on the wafer surface through a Silicon Nitride (SiN) passivation layer, previously deposited to protect the surface during the fabrication process. Gate foot definition is achieved through a PMMA opening to mask the SiN layer plasma etch and the subsequent Ni/Pt thin metal deposition inside that opening by a lift-off procedure. Several different Gate foot L_G openings (250nm, 150nm and 80nm) have been applied in the same wafer on different fabricated devices, to compare the Gate length variation effects on the DC and RF performances. The subsequent thermal annealing of a thin Ni/Pt metal junction allows to improve the Schottky junction characteristics after this thermal treatment, increasing the barrier high from Φ=0.85eV to Φ=1.15eV, with a simultaneous improvement of the ideality factor from n≈2.4 to n≈1.5 (see Fig. 1), and associated with a very low Gate reverse current leakage (i.e. less than 0.2μA/mm at V_{GS}=-10Volt and less than 1mA/mm at V_{GS}=-100Volt).
A second EBL triple resist mask step defines a "T" shaped Gate "head", by depositing a thick Ni/Au layer on top of the Gate "foot" as shown in the focused ion beam (FIB) cross section in Fig. 2 in the case of L_G=150nm.
The use of an annealing thermal cycle before Gate Head definition avoids its negative effect on Gate metal wire parasitic resistance R_{GG} rise, since R_{GG} has been observed to increase from 90Ω/mm to 135Ω/mm when a similar annealing is applied. The associated measured capacitance is C_{GS}=1.0-1.2-1.6pF/mm for devices with L_G=80-150-250nm Gate footprint lengths respectively.

The wafer fabrication ends with the overlay and thick Au metal deposition. A typical maximum Drain current of I_{MAX}=900mA/mm with a maximum transconductance of g_m^{MAX}=310mS/mm has been achieved.

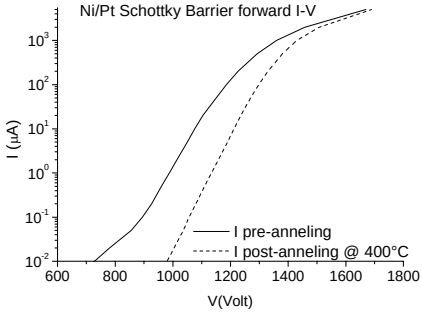

Fig. 1: Ni/Pt Gate foot forward biased IV characteristics before and after the annealing process.

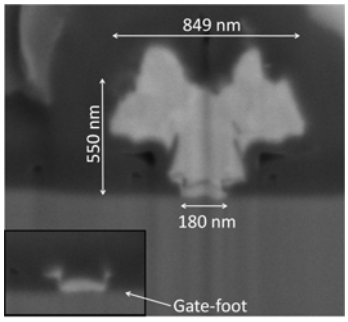

Fig. 2: FIB Gate section image of a double EBL step GaN HEMT, after the foot (insert) and the head metals deposition.

3. RF CHARACTERIZATION

An extensive S-parameter characterization has been performed on L_G=250-150-80nm GaN HEMTs with 10x100µm, 8x75µm and 4x75µm Gate periphery, and the results for W_G=600µm devices are reported in Figure 3: maximum gain performances are achieved on L_G=150nm devices, since the L_G=80nm device transconductance g_m decreases and output conductance $1/R_{DS}$ increases as a consequence of the enhanced short channel effect. A direct consequence of the low R_{GG} value achieved is the limited RF gain degradation while increasing Gate periphery W_G since, by considering L_G=150nm HEMTs, measurements on 4x75µm (typically adopted to design LNAs), and on 10x100µm (typically adopted for Wide-Band HPAs), show an f_T of circa about 46GHz and 38GHz respectively, while f_{Max} results in 92GHz and 72GHz.

Through a cold-source pull test-bench, noise performance has been extracted on 4x75µm FET with L_G=250nm, biased at V_{DS}=15V and I_{DS}=15% I_{DSS}. Such characterization reveals at 15GHz a value of NF_{Min}=0.8dB and Gav=8.7dB. The uncertainty associated to such result, achieved by an innovative test bench, is related to the wide bandwidth of the noise figure meter receiver, and its quantification is on the way [6].

Device power performances from Load-Pull (LP) characterization of W_G=750µm device, biased at V_{DS}=25V at 3dB power compression, show a P_{OUT}=6.3W/mm with G_{ASS}=17dB and PAE=45% (@3GHz), while the saturated output power is P_{OUT}=7.4W/mm (see Fig. 4).

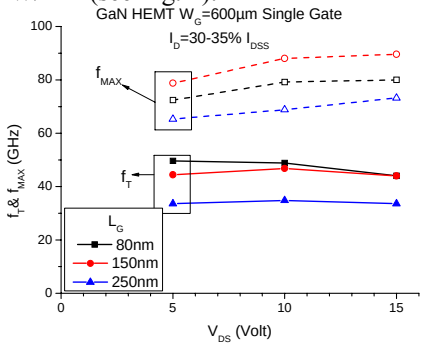

Fig. 3: f_T and f_{MAX} Vs. V_{DS} for various L_G on a W_G=8X75µm=600µm GaN HEMT.

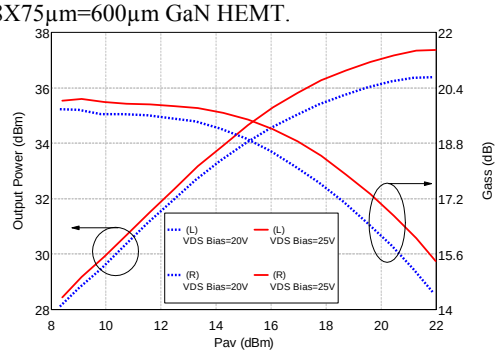

Fig. 4: W_G=750µm L_G=250µm GaN HEMT LP performances at 3GHz, V_{DS}=20V (slashed) and V_{DS}=25V (continuous).

4. CONCLUSIONS

The work illustrates the performances achieved from a GaN HEMT L_G≤250nm new fabrication technology, based on a two Electron Beam Lithography process steps to define the Gate footprint, allowing the thermal annealing of a thin Ni/Pt metal junction, before the second EBL step defining a low resistance Ni/Au Gate head.

Excellent results in terms of noise and output power performance, associated with an high RF gain, has also been demonstrated.

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IMPACT OF Ar-MILLING ON THE GaN SURFACE AND CORRELATION WITH ELECTRICAL RESULTS ON AlGaN/GaN HEMTs

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ABSTRACT

The influence of Argon (Ar)-milling and hydrochloric acid (HCl) treatment on GaN was investigated using x-ray photoelectron spectroscopy (XPS). Furthermore the impact of the pretreatments on electrical performance of AlGaN/GaN high electron mobility transistors (HEMTs) was investigated.

Fluorine (F) residues from plasma etching processes were identified.

Ar-milling removes F-ions and thereby improves drain currents of the HEMTs by approximately 5 % and reduces leakage to about 10 %. Ar-milling increased the Schottky barrier height by approximately 0.05 eV compared to the HCl-dip samples and improved the ideality factor by approximately 0.3.

Additionally pinch-off shifted to an approximately 0.5 V lower gate-source potential.

1. INTRODUCTION

Oxide removal before Schottky metal deposition is a standard surface preparation technique in III/V semiconductor processing. Physical as well as chemical cleanings can be used for this purpose.

Ar-milling and HCl-dip preparations were investigated using the United Monolithic Semiconductors (UMS) 250 nm MMIC technology [1] which uses a passivation assisted gate process.

This process uses a fluorine-based plasma to define the gate foot opening [1]. Therefore chemical properties of the surface layer were investigated by XPS studies to determine possible impacts of this plasma.

Fluorine is also used to fabricate enhancement-mode AlGaN/GaN HEMT devices [2]. Therefore a possible impact of this plasma process on DC characteristics was investigated using two different types of process control monitor structures.

2. EXPERIMENTAL

For this study two GaN on SiC three inch wafers with 29 % Aluminum (Al) concentration in the AlGaN layer and an undoped GaN cap layer were chosen.

This study was split into three steps:

- XPS investigation after plasma etching
- XPS investigation within a process sequence ending with Ar-milling or HCl-dip, respectively
- Comparison of the XPS results with electrical results on HEMT structures with Ar-mill and with HCl-dip preparation

The first wafer was laser-diced into 1 cm^2 samples.
XPS was used on the obtained samples as a surface sensitive technique to identify F-residues from fluorine-based plasma etching.

Lift-off processes after plasma processing were simulated on these samples using a 10 min dip in N-Methyl-2-pyrrolidon (NMP) followed by a de-ionized (DI) water rinse. Afterwards on one sample an HCl-dip followed by a DI water rinse was carried out; on the other sample 180 s Ar-milling was performed.

The second wafer was regularly processed at UMS. Half of this wafer obtained an HCl-dip before gate metallization; the rest was prepared by 180 s in-situ Ar-milling.

From measurements on $1.57*10^{-2}$ mm^2 diodes Schottky barrier height and ideality factor were extracted. For transistor characterization HEMT devices without field plate, 100 µm gate width, a gate source distance of 0.8 µm and a gate drain distance of 3.7 µm were chosen. For the diode and the 3-terminal DC-characterization a Keithley 4200 characterization system was used.

3. RESULTS AND DISCUSSION

3.1. XPS investigation

Due to the time wise split of the experiments it was necessary to normalize the quantitative results from the XPS measurements. The Al-signal of the epitaxially grown AlGaN-layer was found to give an excellent reference for this purpose making the results from different measurement campaigns comparable.

A decreased layer thickness of the GaN-cap would lead to wrong measurement results by an increased reference signal. By 60 s in-situ Ar-milling of the samples in the XPS tool the thickness of the GaN-cap was reduced. By measuring very similar values for the Ga/Al and the N/Al ratio for Ar-milling and HCl-dip it was shown that both pre-treatments had no or the same impact on the thickness of the GaN cap layer. Thus it was shown that normalizing on the Al-counts is a feasible approach.

Fig. 1 shows the normalized F-content of the samples giving a semi-quantitative insight on the concentration at the semiconductor surface.

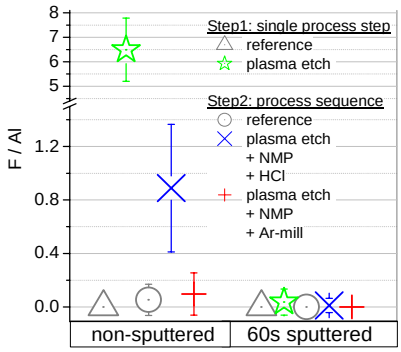

Fig. 1: Fluorine concentration on the GaN-cap surface before and after removing the very surface.

The measurement result after removing the first few monolayers by sputtering the sample with Ar-ions shows that there is either no or only a very limited penetration of F-ions into the cap-layer.

The amount of F-ions from the plasma etch is shown to decrease during processing. Standard processing already decreases the concentration by an order of magnitude. Nevertheless, replacing the HCl dip by an Ar-milling step almost decreases the concentration to the reference values.

3.2. Electrical characterization of HEMT structures

Diode measurements on the fully processed wafer show an increase in Schottky barrier height of about 0.05 eV and an improvement in the ideality factor 0.3 as shown in Fig. 2. However, the spread of the measured values largely increases with Ar-milling.

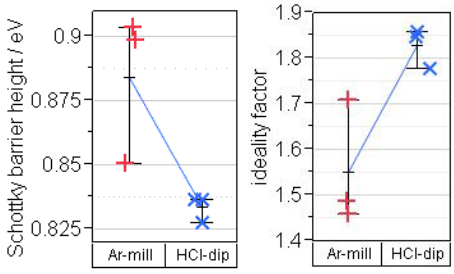

Fig. 2: Impact of surface treatment before metallization on Schottky barrier height and ideality factor

DC measurements on HEMT devices show an increase in drain current of about 5 % for a fully open gate at a gate-source voltage V_{GS} = 1V and a drain-source voltage V_{DS} of 7 to 10 V as shown in Fig. 3.

The presence of negatively charged F-ions at the Schottky interface of the HEMTs with HCl pre-treatment leads to an earlier pinch-off which can be seen in Fig. 4. Additionally leakage currents were reduced by an order of magnitude using the Ar-milling treatment (Fig. 4). Possibly the lower barrier height of the HCl-dip prepared Schottky contact (Fig. 2) contributes to this finding.

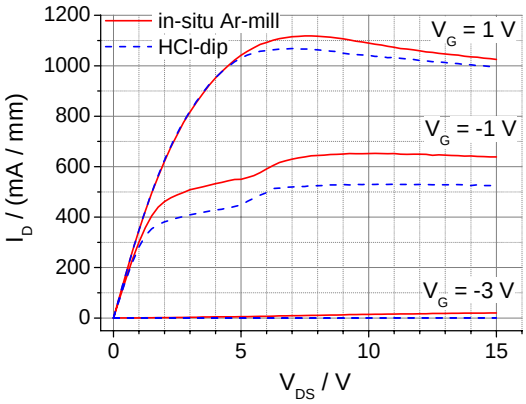

Fig. 3: Transfer characteristics of transistors with different pre-treatments before Schottky deposition.

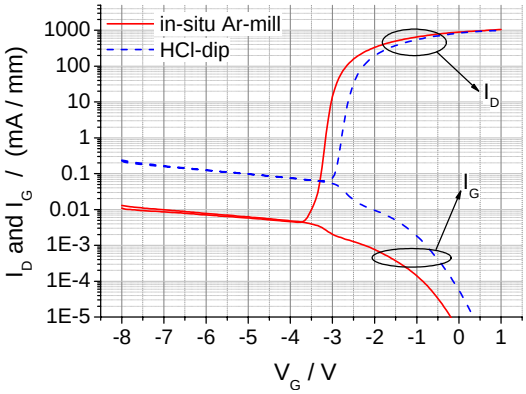

Fig. 4: Pinch-off characteristics of transistors with different pre-treatments before Schottky deposition.

4. CONCLUSIONS

In this study the impact of two different methods of surface cleaning before Schottky deposition after fluorine based plasma etching on the GaN cap surface and the impact on the transistor behavior was investigated.

A positive impact regarding leakage currents and drain currents was observed after F-ion removal by Ar-milling before deposition of the gate contact.

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IMPACT OF GATE LENGTH ON THE DEVICE PERFORMANCE OF PASSIVATED InAlN/GaN HFET

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ABSTRACT

In our study, InAlN/GaN heterostructure field effect transistors (HFETs) with an 8.3 nm thick nearly lattice matched barrier layer are investigated. The devices are passivated with PECVD SiN and the gate length L_G varies from 75 nm to 2 µm. The measured peak value of the extrinsic transconductance $g_{m,ext}$ in DC operation is 460 mS/mm. For the L_G = 75 nm device, current and gain cut-off frequencies are as high as f_T = 100 GHz and f_{MAX} = 140 GHz, respectively. The DC and RF parameters scale with the gate length as expected, although short channel effects are already observed for devices with gate lengths as high as 110 nm.

1. INTRODUCTION

In recent years, GaN based Heterostructure Field Effect Transistors (HFETs) were subject to intense research efforts. Especially InAlN based heterostructures have moved into focus of investigation due to their outstanding potential for radio frequency applications. Nevertheless, downscaling of the device geometries is a vital requirement to reach high current gain cut-off frequencies f_T. For the AlGaN/GaN counterpart the scaling behaviour of the device DC and RF parameters have already been investigated intensely [1, 2]. Short channel effects are known to dominate frequency response for gate length to barrier thickness aspect ratios lower than 15. In this paper it is demonstrated that the model for the f_T of AlGaN/GaN HFETs proposed by Jessen et al. [2] is transferable to InAlN/GaN HFETs in its general outline. Only minor changes in the extracted parameters, mainly due to higher sheet carrier density and smaller effective electron velocity in our devices, have to be made.

2. FABRICATION AND MEASUREMENT

A nearly lattice matched InAlN/GaN heterostructure with a barrier thickness of 8.3 nm has been grown on sapphire substrate by MOCVD in an *AIXTRON SE* close coupled showerhead reactor. For transistor fabrication common processing techniques have been applied, including mesa isolation by chlorine based plasma etching or ion implantation, evaporation of Ti/Al/Ni/Au and Ni/Au for the ohmic and gate contacts, respectively, RTA annealing and SiN deposition of the passivation layer by plasma enhanced chemical vapor deposition. A double finger gate geometry with a total gate width of 2 x 50 µm was processed with gate length ranging from 75 nm to 2 µm, realized by e-Beam lithography on comparable wafers.

DC and RF characterization was performed for all devices. Current and gain cut-off frequencies were determined by extrapolation from S-parameter measurements.

3. RESULTS AND DISCUSSION

The different device geometries as well as DC and RF measurement results are summarized in table 1.

Table 1
Device identification with gate length L_G, source gate spacing L_{SG}, aspect ratio gate length to channel separation, source resistance R_S, maximum transconductance $g_{m,max}$, current gain cut-off frequency f_T, product of f_T and L_G, threshold voltage V_{th} of the devices for a drain voltage of 10 V

Device ID	L_G [µm]	L_{SG} [µm]	L_G/t_{bar}	R_S [Ωmm]	$g_{m,max}$ [mS/mm]	f_T [GHz]	f_T x L_G [GHz µm]	V_{th} [V]
A	2	1	241	0.99	260	6.7	13.4	-3.1
B	1	1.5	120	1.09	299	14.1	14.1	-3.2
C	0.5	1.5	60	1.09	369	26.3	13.2	-3.2
D	0.225	0.76	27	0.73	424	52	11.7	-3.6
E	0.110	0.82	13	1.01	231	80	8.8	-4.8
F	0.075	0.84	9	0.75	248	100	7.5	-5.5

Additionally, the mean value for the source resistance R_S for each device is given. It has been calculated from transfer-length-method (TLM) results and the source gate spacing L_{GS} ($R_S = R_C + L_{SG} \times R_{SH}$). The sheet resistance R_{SH} measured by TLM and van-der-Pauw is 190 Ω/o.

Fig 1 presents the transfer characteristics of all devices. Even for gate lengths above 0.5 µm (devices A, B and C) the current scales much weaker than with 1/Lg. This indicates that the intrinsic electric field is not solely relevant for the drain current, but that velocity saturation effects are also relevant. A closer analysis of extracted intrinsic parameters may shed more light into this observation.

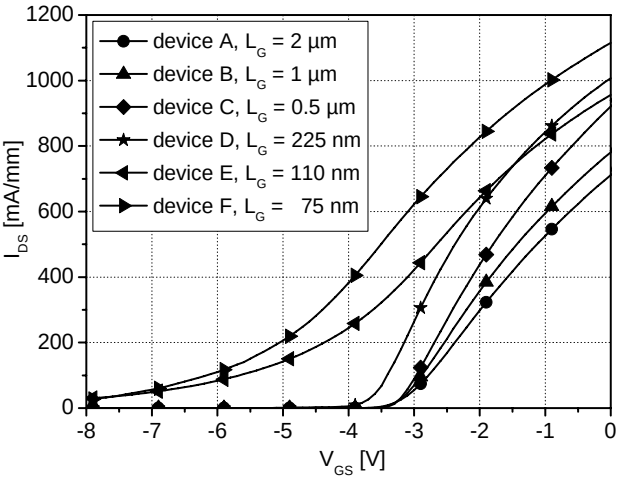

Fig 1: Transfer characteristics of InAlN/GaN HFETs with different gate length L_G

Comparison of the drain current below the threshold voltage shows a dramatic increase with smaller gate length. Even the threshold voltage itself shifts to more negative values. The modulation efficiency of the channel decreases due to the smaller gate length to barrier thickness aspect ratio. This smaller aspect ratio leads to an increased drain induced electric field parallel to the channel and therefore weakens the influence of the applied gate voltage. This effect can also be seen in the maximum transconductance $g_{m,max}$. Initially it increases with smaller gate length, but for the devices E and F it drops significantly.

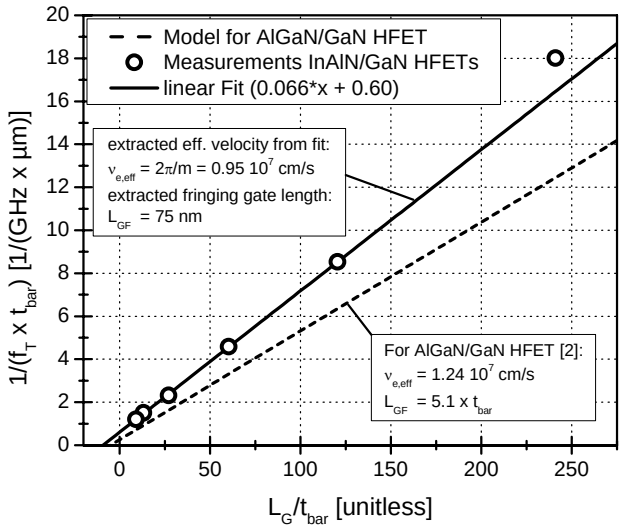

Fig 2: $1/(f_T \times t_{bar})$ as a function of L_G/t_{bar}. The fit corresponds to formula (1) and is used to extract ν_{eff} and L_{GF}.

The effective gate length $L_{G,eff}$ and the extrinsic effective carrier velocity ν_{eff} can be extracted from [2]:

$$\frac{1}{f_T \cdot t_{bar}} = \frac{2\pi}{\upsilon_{e,eff}}\left(\frac{L_G}{t_{bar}}\right) + \frac{2\pi}{\upsilon_{e,eff}}\left(\frac{L_{GF}}{t_{bar}}\right) \qquad (1)$$

where L_{GF} accounts for the fringing effect at the gate edges ($L_{G,eff} = L_G + L_{GF}$). In fig 2 the corresponding plot and the fit of the measurement points are given. From the fit an effective extrinsic electron velocity ν_{eff} of 0.95×10^7 cm/s and a fringing gate length L_{GF} of 75 nm can be extracted for our devices. For comparison, the extracted model for AlGaN/GaN HFETs is also given [2], which predicts a ν_{eff} of 1.24×10^7 cm/s and an L_{GF} of $5.1 \times t_{bar}$.

The extracted values demonstrate that for InAlN/GaN slight changes to the model parameters have to be applied. Further studies will have to confirm, if our extracted values are generally valid for InAlN HFETs.

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THRESHOLD VOLTAGE SCALING IN E-MODE InAlN/AlN-GaN HEMTS ON Si SUBSTRATES

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ABSTRACT

In this work we present enhancement-mode (E-mode) GaN high electron mobility transistors (HEMTs) on Si substrates with ZrO_2 gate dielectrics of different thicknesses. The oxide interlayers between the barrier and gate metal allow raising the already positive threshold voltage of the device, controlled by the thickness of the oxide layer. Additional advantages of the interlayer are a reduced gate leakage current and an increase of the drain current on/off ratio.

1. INTRODUCTION

In order to use GaN high electron mobility transistors (HEMTs) for digital or power switch applications, normally-off devices on a Si substrate with minimal gate leakage current are required. It is possible to achieve a positive threshold voltage with the reduction of the InAlN/AlN barrier thickness. Scaling of the barrier thickness and its influence on the threshold voltage was analyzed in Ref. [1]. According to the model a positive threshold voltage should be obtained for a barrier thickness of less than 3 nm. This was achieved in previous works with GaN HEMTs on sapphire substrates, using Schottky-barrier gates [2] with a 2 nm thin InAlN/AlN barrier, so the conduction band minimum in the channel is raised above the Fermi-level. The threshold voltage of these transistors was below 1 V and they exhibited high gate leakage current.
In this work we enhance this device design by adding an oxide gate dielectric in order to further increase the threshold voltage. The oxide does not have inherent spontaneous polarization, so the severe scaling rules for barrier thicknesses [1] can be circumvented.

2. EXPERIMENT

The heterostructures are grown on Si substrates and consist of a GaN buffer, a 2 nm thin InAlN/AlN barrier and a 6 nm thick n^+-doped GaN cap. The cap layer is passivated by 100 nm SiN. In the gate region, the SiN passivation and the GaN cap layer are recessed by reactive ion etching (RIE). ZrO_2 of various thicknesses (10, 12, 18 and 24 nm) is deposited by atomic layer deposition (ALD) before gate metallization. The gate length is 1 µm, the width 25 µm. On these devices transfer and output characteristics have been measured.

3. RESULTS AND DISCUSSION

Typical transfer and output characteristics of a device with 10 nm ZrO_2 are shown in Fig. 1 and Fig. 2 respectively. The device exhibits a threshold voltage of 2.3 V and a maximum drain current of about 0.45 A/mm. The maximum transconductance is 140 mS/mm.
The devices with increased oxide layer thicknesses exhibit lower drain currents: 0.33 A/mm, 0.28 A/mm and 0.25 A/mm for 12, 18 and 24 nm respectively. This is due to the fact that the influence of the polarization charge of

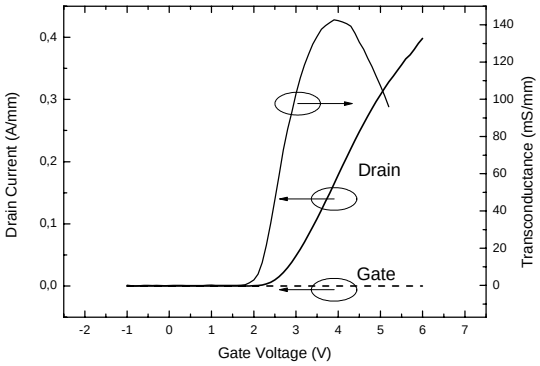

Fig. 1: Transfer and transconductance characteristic of a GaN HEMT with 10 nm ZrO_2 between InAlN barrier and gate metal.

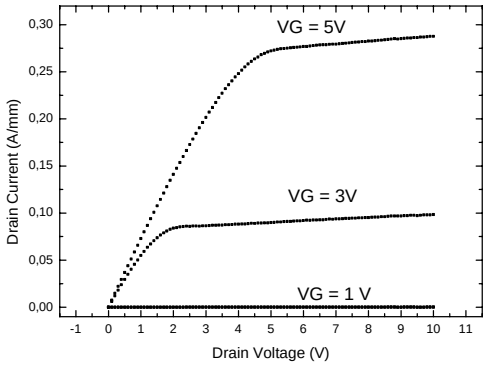

Fig. 2: Output characteristic of a GaN HEMT with 10 nm ZrO_2 between InAlN barrier and gate metal.

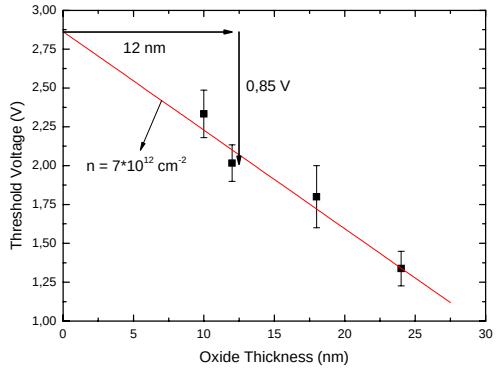

Fig. 3: Measured (symbols) threshold voltage dependence on the oxide thickness. The line is a linear fit to the data. The total density of interface charges is estimated to n = $7x10^{12}$ cm^{-2}.

the 2 nm thin InAlN/AlN barrier decreases with higher oxide thickness, which leads to a lower 2DEG carrier concentration. For all devices the gate leakage current is below 100 nA/mm, which is 6 orders of magnitude lower compared to the Schottky-barrier device in [3]. The gate voltage swing is up to 10 V and the drain current on/off ratio is up to 4 orders of magnitude.

The threshold voltage shows a nearly linear dependence on the thickness of the oxide layer (fig. 3). It varies between 1.3 V and 2.3 V for the samples with a 24 nm and a 10 nm thick oxide respectively. The extrapolation of the linear threshold voltage dependence to zero voltage gives a value of 2.9 V, which is different from the measured 0.3 V without the oxide [3]. The difference is interpreted as due to negative fixed charge at the interface between ZrO_2 and InAlN/AlN barrier. Using the slope of the linear fit, the interface trap density has been estimated to n = $7x10^{12}$ cm^{-2}. Hence the combination of fixed interface charge and variation of oxide layer thickness can explain the linear correlation to the threshold voltage.

Consequently the question arises, if a further reduction of the oxide thickness is reasonable. On the one hand an even higher threshold voltage could be achieved, according to the linear model, while higher maximum drain currents are expected. On the other hand advantages compared to the Schottky-barrier devices get lost, since it is estimated that the gate current leakage will increase again. It is unclear if the model will uphold its linearity for thinner oxide layers due to the above mentioned gate current leakage.

4. CONCLUSIONS

GaN HEMTs on Si substrates with a ZrO_2 gate dielectric of different thicknesses were built. The devices show E-mode operation and their threshold voltages are between 1.3 V and 2.3 V. For the measured devices with 10, 12, 18 and 24 nm oxide layers the threshold voltage shows a linear dependence on the oxide thickness. The threshold voltage increases with decreasing oxide interlayer thickness. This effect is related to the fixed charge at the interface between oxide layer and InAlN barrier. A thinner oxide layer provides higher threshold voltage and drain current, but also a higher gate leakage. One has to consider these different factors in the design layout.

ACKNOWLEDGMENTS

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ELECTRICAL AND RELIABILITY INVESTIGATION OF AlGaN/GaN HEMTS GROWN ON 8° OFF-AXIS 4H-SiC

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ABSTRACT

In this paper we report on the performances and on the reliability study of AlGaN/GaN HEMTs grown onto misoriented 4H-SiC substrate, 8° off-axis along the [11-20] direction. The substrate's misorientation have produced defects preferentially oriented along the cut direction, limiting the carrier transport along the orthogonal direction. As a consequence, it has been observed a strong anisotropy of the electrical performances between devices processed along the two directions. Despite this different electrical behaviour, the paper will show that device robustness appears not to be influenced by the big defects presence.

1. INTRODUCTION

Gallium Nitride (GaN) and the nitride materials have shown very good intrinsic properties suitable for high-power and high-frequency electronics applications. The presence of a two dimensional electron gas (2DEG) at the AlGaN/GaN interface and the high electric-field robustness of the material, make the heterostructure suitable for high-power high electron mobility devices that can operate from S-band to millimeter-wave range.

The lack of this technology is the absence of defect-free substrates in which devices can be grown. A possible strategy to limit the growth of defects and to improve the heterostructure quality is the use of substrates with a low misorientation angle. In fact, the use of misoriented substrates should enable a better step-flow mechanism during the growth of GaN, and can be a good method to improve the surface flatness, to decrease the dislocation density [1] or to prevent the formation of hillocks on the surface [2]. Matsushita et al. [3] reported that a low misorientation angle on SiC substrates results in a reduction of the current collapse, but also leads to a faster current degradation of HEMTs. On the other hand, Nakamura et al. [4] observed an anisotropy of the Hall mobility in AlGaN/GaN structures grown by molecular beam epitaxy onto off-axis 4H-SiC, due to the presence of oriented macrosteps on the surface.

This paper report on the electrical investigation in AlGaN/GaN HEMTs grown on misoriented 4H-SiC substrates, 8° off-axis along the [11-20] direction. The misorientation of the SiC substrate have created a particular surface morphology characterized by the presence of big defects that are preferentially oriented along the cut direction. The intersection of these defects with the AlGaN/GaN interface have limited the electron flow along the [1-100] direction. For this reason, a strong anisotropy of the channel electrical behaviour has been observed, depending on the orientation of the processed devices. Extensive DC analysis and reliability tests have been performed to verify how these preferentially oriented defects affect reliability performances of the processed devices.

2. DEVICE DESCRIPTION

The wafer studied in this work uses an heavily doped n-type 4H-SiC off-axis substrate, 8° misoriented in the [11-20] direction, with an unintentionally doped 4H-SiC epitaxial layers grown on top by ETC. The AlGaN/GaN heterostructure is formed by a 30nm thick $Al_{0.3}Ga_{0.7}N$ barrier layer and a 1um thick undoped GaN buffer, grown by metalorganic chemical vapour deposition (MOCVD) above the substrate, after a thin AlN nucleation layer.

To determine the electrical properties of the channel, electrical measurements have been performed on test-HEMT devices, with source-drain distance of 20um, gate length of 2um and gate width of 120um (L_{GS}=L_{GD}=9um). Annealed Ti/Al/Ni/Au contacts were used as source and drain electrodes, and Pt/Au bilayer as gate electrode. Device isolation was obtained by a combination of mesa etch and nitrogen ion-implantation.

The HEMTs were fabricated in two different orientations: with the 2DEG channel oriented along the [11-20] direction or along the [1-100] direction.

3. EXPERIMENTAL RESULTS

To evaluate the material quality of the wafer, surface morphology has been characterized with an atomic force microscopy (AFM), using a DI 3100 equipment by Veeco, operating in tapping mode. Furthermore, the sample microstructure has been evaluated with a transmission electron microscopy (TEM), using a 200-kV JEM 2010 JEOL microscope. Fig. 1-a shows the surface morphology obtained by AFM scans over a 5umx5um area of the AlGaN/GaN heterostructure grown onto an 8° misoriented 4H-SiC. As can be seen, macrosteps oriented along the [1-100] are well visible on the AlGaN surface, with a terrace width of 60-80 nm, that can be attributed to the growth on the misoriented substrate.

Fig. 1-b and Fig. 1-c show cross section TEM images of the samples cut, in the [11-20] and [1-100] directions respectively. The sample cut in the [11-20] direction has shown the presence of a rough surface, characterized by undulations of 60-80nm, that are clearly related to the surface macrosteps described above. On the other hand,

the TEM cross section on [1-100] direction has shown the "V-shape" nature of the surface defects.

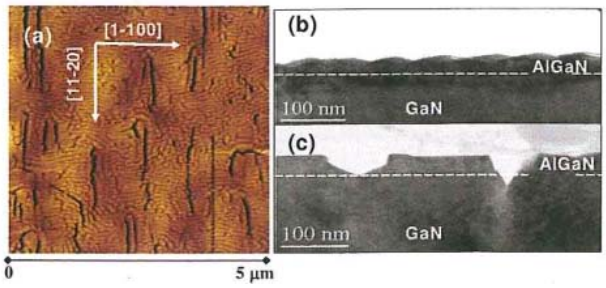

Fig. 1: (a) AFM images of the surface morphology of AlGaN/GaN heterostructure. Cross section TEM images of the samples cut along the [11-20] direction (b) and along the [1-100] direction (c). Dashed line indicates the 2DEG location.

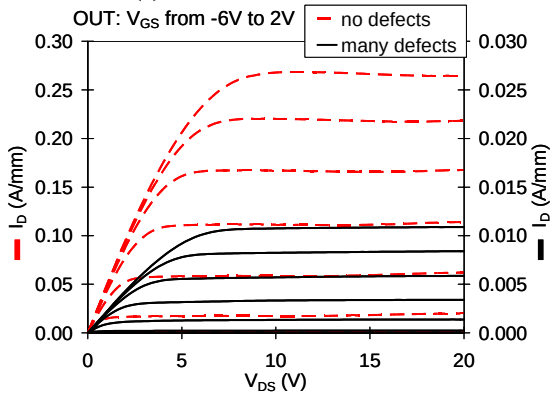

Fig. 2: Comparison between output characteristics of "no defects" devices (channel on [11-20] direction) and "many defects" devices (channel on [1-100] direction).

These defects are distributed on the whole AlGaN surface, with a distance from 200nm to few micrometers; sometimes the defects cross the AlGaN/GaN interface and consequently they affect the 2DEG region.

Clearly, V-defects on the AlGaN/GaN heterointerface and surface roughness are expected to influence the 2DEG electrical properties and the scattering phenomena. In order to determine the influence of the material quality on the electrical properties of the 2DEG, electrical measurements have been carried out on test-HEMT devices processed with two different channel orientations: parallel to the dislocations ([11-20] called "no defects") and orthogonal to the dislocations ([1-100] called "many defects"). The I-V characteristics of HEMT devices with electron channel parallel to [11-20] direction have shown better electrical performances (drain current difference of more than one order of magnitude) compared to devices processed on the orthogonal direction (see Fig. 2).

To investigate the reliability behaviour of these devices, characterized by a strong difference on the defect concentration on the active area, several reverse bias step-stress have been performed on devices with different orientation and on different wafer's areas. These tests consist in reverse biasing the gate terminal at higher voltages step by step, keeping the drain and the source terminal to ground, in order to study the high-electric field robustness of gate diodes. In particular we have used step of 10V, 2 minutes long. At the end of each step, DC characterization and few emission microscopy images have been performed, to check the presence of strange spots in ON-state or in OFF-state conditions.

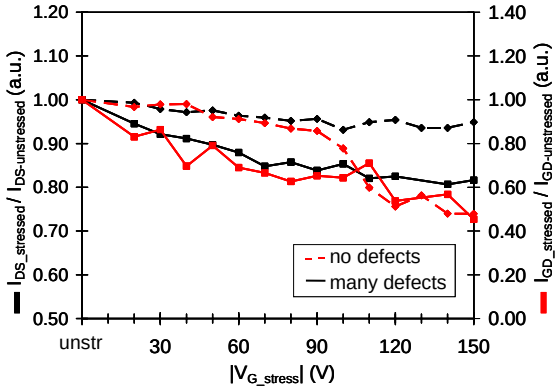

Fig. 3: Transistor I_{GD} diode leakage (at V_{GD}=-8V) and I_{DS} current (at V_{GS}=0V, V_{DS}=20V) variation during reverse bias gate step stress, with V_G from -20V to -150V.

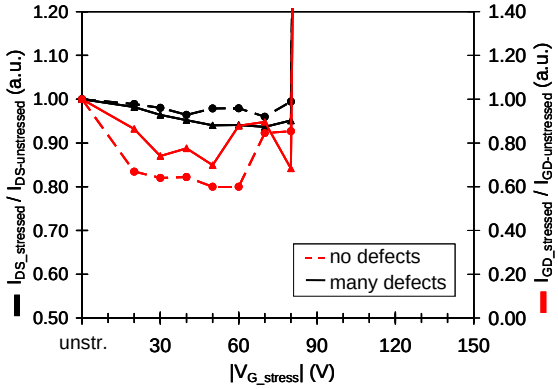

Fig. 4: Transistor I_{GD} diode leakage (at V_{GD}=-8V) and I_{DS} current (at V_{GS}=0V, V_{DS}=20V) variation during reverse bias gate step stress, failed at V_G = -80V.

But results have shown degradation mechanisms not so correlated with the different device's orientation.

In particular, few devices in the same wafer area, but with different orientations, have shown very high electric field robustness up to -150V of gate-drain and gate-source voltage, without showing any big electrical degradation or emission variation (see Fig. 3). But other devices with both channel directions, located on another area, have failed instantaneously at about -80V of gate-drain and gate-source voltage, without showing big degradation during the previous steps.

From these results, we can observe that the different defect density on the active area or on the highest electric-field region does not play an important role on device degradation and on diode robustness, in particular using the reverse bias step-stress. The absence of uniform results on similar devices show that wafer position or other processing problems could reduce device reliability.

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Session 9 :

WBG compound semiconductors for power electronics

Chair : Prof. Kostantinos Zekentes

Wednesday June 1, 09:00 - 10:20

RECENT ADVANCES IN HIGH-VOLTAGE GaN MOS-GATED TRANSISTORS FOR POWER ELECTRONICS APPLICATIONS

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ABSTRACT

The recent progress and present status of the development of high-voltage lateral power GaN field-effect transistors for power switching applications are reviewed and discussed. The basic device structures explored and the performance improvement in blocking voltage and specific on-resistance over the last few years are presented. The technical challenges and reliability issues that still need to be addressed are pointed out.

1. INTRODUCTION

Similar to SiC, GaN has many attractive material properties, such as high breakdown field, good bulk electron mobility and thermal conductivity, which make it suitable for high power switching as well as high frequency amplifying electronic applications [1] (see Table I). On the other hand, thin layers of GaN have been successfully heteroepitaxially grown, with suitable AlN/GaN buffer layers, on silicon, sapphire and SiC substrates. In addition, GaN has demonstrated two-dimensional electron gas (2DEG) at heterojunction interfaces (AlGaN/GaN, AlInN/GaN) that has very high electron mobilities (~2000cm2/V-s). Furthermore, the fabrication processing steps for GaN devices have thermal budgets that are compatible with state-of-art silicon nanometer CMOS foundries and can exploit these infrastructures for cost-effective, large-scale GaN power device commercialization and manufacturing.

Table I: Semiconductor properties

Material	E_g (eV)	*Direct/ Indirect*	n_i (cm^{-3})	ε_r	μ_n (cm^2/V-s)	E_c (MV/cm)	v_{sat} (10^7 cm/s)	λ (W/cm-*K*)
Si	1.1	I	$1.5x10^{10}$	11.8	1350	0.3	1.0	1.5
2H-GaN	3.39	D	$1.9x10^{-10}$	9.9	1000[a] 2000**	3.3*	2.5	1.3
3C-GaN	3.27	D	$8x10^{-9}$	9.9	1000	1*	2.5	1.3
3C-SiC	2.2	I	6.9	9.6	900	1.2*	2.0	4.5
4H-SiC	3.26	I	$8.2x10^{-9}$	10	720[a] 650[c]	2.0	2.0	4.5
6H-SiC	3.0	I	$2.3x10^{-6}$	9.7	370[a] 50[c]	2.4	2.0	4.5

Note: a – mobility along a-axis, c-mobility along c-axis, *Estimated value, **2DEG

A few years ago, discrete RF GaN power HEMTs on silicon substrates as well as high-voltage discrete power GaN Schottky diodes (600V, 4 to 8A) on sapphire substrates have been commercialized [2-4]. More recently, high voltage (200V, 12A) GaN power transistors on silicon substrates are becoming commercially available [5,6].

In this paper, we will present the recent advances in high-voltage GaN power transistors. These transistors can function both as discrete power switches or integrated with other logic or analog device elements to form power ICs.

2. DEVICE STRUCTURES AND DESIGN

Most of the high-voltage GaN power transistors reported are lateral in structure because the GaN/AlGaN epitaxial layers are grown on insulating or high resistivity substrates. The schematic cross-sections of several high-voltage lateral GaN transistor structures are shown in Figs. 1a-d. Power GaN transistors are interesting in that they can either resemble that of lateral silicon power MOSFETs or AlGaAs/GaAs Schottky-gate HEMTs. Besides a MOS channel, lateral high-voltage GaN MOSFETs have a lightly doped drain region to support high drain voltages and ion-implanted source/drain regions. By contrast, power AlGaN/GaN HEMTs have Schottky-gate controlled heterojunction 2DEG channel, a heterojunction drift region and alloyed source/drain contacts. In either type of transistors, the surface electric field must be suppressed so as to maximum the blocking voltage. The MOS Channel-HEMT (MOSC-HEMT, previously called hybrid MOS-HEMT [7]) combines the best features of the MOSFET and HEMT.

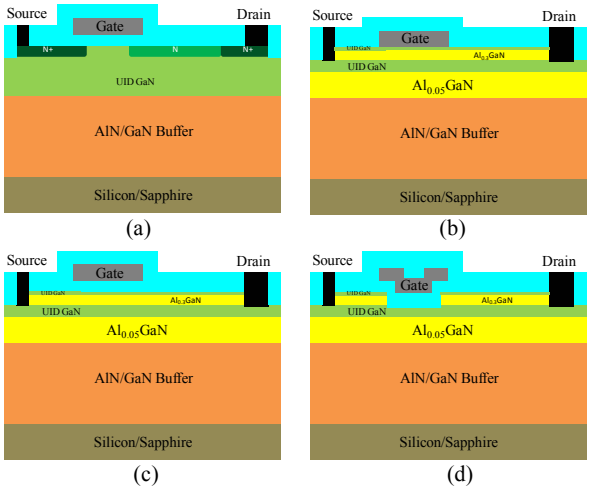


Fig. 1: Schematic cross-sections of high voltage lateral GaN (a) MOSFET (b) HEMT (c) MOS-HEMT and (d) MOS-channel HEMT (MOSC-HEMT)

3. DEVICE DESIGN

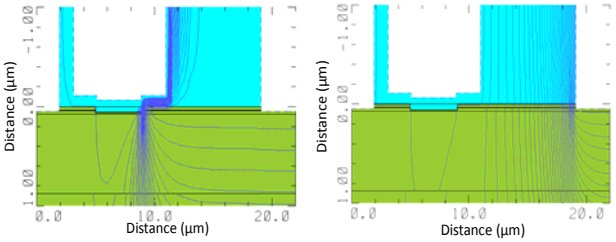
The REshaping of SUrface Field (RESURF) principle [8] is employed to maximize the breakdown voltage of lateral high-voltage power devices since it can suppress the surface electric field and force the avalanche process to be initiated in the bulk junction region. The key design parameter is the space charge per unit area (N_{RESURF}) ($= \int N_{epi}\, dx$) in the drift region. Adoption of an optimum N_{RESURF} leads to inherent lateral and vertical electric field shaping due to non-planar, two or three dimensional depletion action originating from interactions of lateral and vertical pn or MIS junctions [9-11].

To determine the optimum RESURF charge density (N_{RESURF}), we use Gauss' Law to yield

$$\int \xi \cdot dA \approx \xi \cdot A = -\int \rho\, dV / \varepsilon_s = -Q / \varepsilon_s = -q N / \varepsilon_s$$

where ξ is the electric field in the depleted drift region, A the area, Q the total amount of space charges enclosed and ε_s the semiconductor permittivity. Since $N_{RESURF} = Q_{RESURF} / q A \approx \xi \varepsilon_s / q$ and $\xi \approx 1.5\times10^5$V/cm in silicon, the optimum N_{RESURF} is about 10^{12}/cm^2, but, for GaN and SiC, where the avalanche field is 10 times higher, it is 10^{13}/cm^2. Additional features, such as field plates, are needed to further reduce surface field crowding, either near the gate/source or drain side of the device. In addition, the RESURF action can be achieved in many ways: (a) space charge can be introduced with in situ epi doping, ion implantation or polarization charges, and (b) the substrates can be semiconductors (like Si or GaN), insulators (like sapphire) or semiconductor on insulator/semiconductor (SOI) structures (like silicon/oxide/silicon or GaN/AlN/silicon). Here, we are focusing on lateral GaN power devices on SOI substrates consisting of AlGaN/GaN or GaN active epitaxial layers/AlN, GaN or AlGaN insulating buffer layers on silicon substrates. Interestingly, the space charges in the AlGaN/GaN case arise from polarization charges and with an aluminum mole fraction of about 22% and an AlGaN/GaN layer thickness of 20nm, these polarization charges are about 10^{13}/cm^2 in concentration [12]. Consequently, such a structure can be called a "natural" RESURF structure, and, in the case of infinite number of parallel RESURF layers, a natural superjunction structure [13]. To illustrate the impact of balanced space charges in the drift region, we have simulated two structures, one with uncompensated positive charges at the AlGaN/GaN interface and the other with balanced positive and negative charges on the two AlGaN interfaces. The equipotential line profiles, shown in Fig. 2, clearly indicate field crowding at the gate corner in the former but much more uniform electric field in the latter [14].

While employment of the RESURF approach results in minimum drift region length for a given breakdown voltage (BV), it also leads to a minimum specific on-resistance ($R_{on,sp}$) . In particular, using an one-dimensional pn junction breakdown theory, one deduce a $R_{on,sp} \propto (BV)^{2.5}$ relationship for unipolar rectifiers or transistors and we almost always find this relationship to



(a) (b)

Fig. 2: Simulated equivalent potential line distribution for 1-zone RESURF MOSC-HEMT (a) without GaN cap at V_{DS} of 40V and (b) with GaN cap at V_{DS} of 646V

be applicable in vertical discrete devices. By contrast, lateral RESURF-type unipolar devices have a $R_{on,sp} \propto (BV)^n$, where n is between 1.1 and 1.5, significantly smaller than that of vertical devices. In addition, for power FET structures, we also need to consider the on-resistance component (R_{ch}) contributed from the channel region and this resistance is directly related to the field-effect carrier mobility achievable from a particular FET process. The relative on-resistance contributions from the channel and drift regions are strongly dependent on the blocking or breakdown voltage desired. In 600V lateral silicon RESURF devices, the drift region resistance dominates. However, in lateral GaN RESURF devices of the same blocking voltage, the on-resistances from the MOS channel, relative to the resistance of the drift region, is becoming increasingly dependent on the channel length and field-effect mobility. Consequently, the choice of channel region design and technology in GaN power FETs plays a major role in ultimate device performance and proper channel scaling is necessary and critical with blocking voltages below 600V. To illustrate these

Table II: Device parameters for lateral GaN MOSFETs in calculating the breakdown voltage/on-resistance tradeoff

L_G (μm)	$n_{s,CH}$ (cm^{-2})	μ_{CH} (cm^2/V-s)	E_{RES} (V/μm)	Φ_{RES} (cm^{-2})	μ_{RES} (cm^2/V-s)
3	1×10^{13}	540	100	1×10^{13}	900

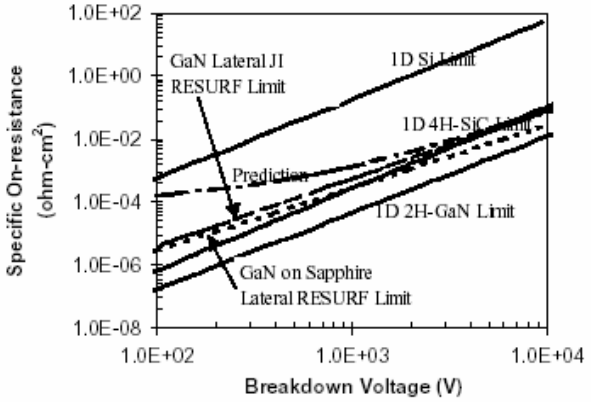


Fig. 3: Projections of the performance of GaN devices

considerations, the specific on-resistance vs. blocking voltage for GaN MOSFETs, using the set of device and material parameters assumed in Table II, is shown in Fig. 3 [15]. Also, included for comparison is the one-

dimensional bulk vertical GaN device performance projection.

For power MOSC-HEMTs, the channel resistance has become so dominant that scaling it to below submicron dimensions is necessary. We have performed a systematic channel scaling study and found that scaling the channel length to below 1μm is needed to achieve specific on-resistance below 10mΩ-cm^2 [16], as shown in Fig. 4. It can also be noted that the $R_{on,sp}$ of the conventional HEMTs is less sensitive to the channel length because of a higher channel mobility, but it is more difficult to achieve a sufficiently large positive threshold voltage for enhancement mode operation.

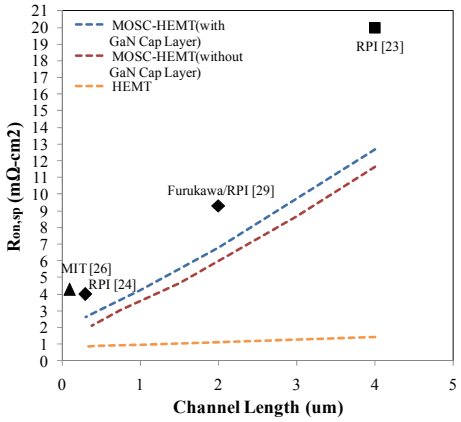


Fig. 4: $R_{on,sp}$ vs. MOS channel length from experiments and simulations for HEMT and MOSC-HEMT without or with GaN cap layer

3. EXPERIMENTAL RESULTS

The first high voltage GaN power transistor is a MOS-HEMT on sapphire, with a $R_{on,sp}$ of 1.7mΩ-cm^2 and a BV of 1.3kV [17]. Subsequently, there are many attempts to refine the device structures and process to improve its characteristics. The main structural variants include insertion a better dielectric between the Schottky metal and AlGaN layer, varying Al mole fraction in the AlGaN layer and better surface passivation layer. The device parameters optimized are: BV, off-state leakage current, gate leakage and frequency-dependent current dispersion. However, most of the off-state leakage current reported are often excessive (usually, the BV was measured at 1mA/mm) [18]. Recently, the situation has been improved, and, in one case, accomplished with an *in situ* grown surface SiN passivation layer [19]. The highest BV for a GaN HEMT reported is 10.4kV, with a specific on-resistance of 186 mΩ-cm^2 [20]. It is interesting to note that all the high-voltage commercial GaN power transistors so far base on the basic HEMT device structure approach, though mostly on silicon substrates [5,6].

While most of the GaN transistors demonstrated utilized a heterojunction channel and Schottky (sometimes in conjunction with a dielectric) gate (see Table III), we have focused on developing an enhancement mode MOS channel technology. Previously, we have successfully

Table III: Summary of GaN high voltage transistors

Device	BV (V)	$R_{on,sp}$ (mΩ×cm^2)/ Imax(A)	Other Features	Research Group /Company	References
HEMT	1300	1.7	SiO_2 /Si_3N_4 as gate insulator L_{GD}=20um	UCSB	N.Q.Zhang et al., IEDM 2001
HEMT	8300	186	L_{GD}=125um, field plate	Panasonic	Y. Uemoto et al., IEDM 2007
HEMT (GIT)	800	2.6	L_{GD}=7.5um, V_{th}=1 V, p-AlGaN/AlGaN under gate	Panasonic	Y. Uemoto et al., TED 2007
HEMT	1800	7, 120A	L_{GD}=15um, Si substrate	Furukawa	N. Ikeda et al., ISPSD 2008
HEMT	1580	4	L_{GD}=16um	Cornell	J. Shi et al., PSS(c) 2008
HEMT	100	300 mA/mm	V_{th}=0.75V, Fluoride plasma treatment	HKUST	D. Song et al., EDL 2007
HEMT	1500	5.3	L_{GD}=20um, Si substrate transfer	MIT	B. Lu et al., EDL 2010
HEMT	2200	18	L_{GD}=20um, Si substrate removal	IEMC	P. Srivastava et al., EDL 2011
HEMT	1100	6.1	L_{GD}=22um	U. of Sheffield /Powdec	A. Nakajima et al., EDL 2011
HEMT	10400	186	L_{GD}=125um, thick poly-AlN passivation	Panasonic	M. Yanagihara et al., PSS(A) 2009
MOSFET	1570	2.5 A	V_{th}=3V, implanted RESURF region	RPI	W. Huang et al., ISPSD 2008
MOSFET		80 mA/mm	V_{th}=5.1V	Rohm	H. Otake et al., JJAP 2007
MOSFET	770 forward 1050 reverse		Monolithic Schottky pair, reverse blocking, L_{GD}=18um	RPI	W. Huang et al., ISPSD 2007
MOSFET	2500		L_{GD}=30um, field plates, lower temperatur anneal	RPI	W. Huang et al., ISPSD 2008
		30	L_{GD}=20um, V_{th}=2 V, higher temperature anneal		
MOSFET	730	34	L_{GD}=16um	RPI	W. Huang et al., ISPSD 2009
MOS-HEMT	1000	5	L_{GD}=15um, V_{th}=0.5V, Si substrate	NEC	K. Ota et al., IEDM 2009
MOS-HEMT	320	800 mA/mm	L_{GD}=5um, V_{th}=3V, Lch=0.8um, GaN/AlN/GaN cap	Fujits	M. Kanamurua et al., EDL 2010
MOS-HEMT	1200	9	L_{GD}=5um, V_{th}=0.64V, plasma treated gate	HRL	R. Chu et al., EDL 2011
MISC-HEMT	640	3.8	L_{GD}=12um, V_{th}=1 V	Toshiba	M. Kuraguchi et al., PSS(c) 2007
MOSC-HEMT		20	L_{GD}=20um, V_{th}=2.5 V	RPI	W. Huang et al., ISPSD 2008
MOSC-HEMT	1300		L_{GD}=24um, field plate	RPI	K. Tang et al., ISPSD 2009
MOSC-HEMT	650	9.3, 100A	LGD=15um, V_{th}=2.7V, Si substrate	Furukawa /RPI	Kambayashi et. al. and T.P Chow, SSE 2010
MISC-HEMT	400	200 mA/mm	L_{GD}=6.5um, V_{th}=5.2V, Si substrate	Sharp	T. Oka et al., EDL 2008
MOSC-HEMT	643	4.3	L_{GD}=18um, V_{th}=2.9V, L_{ch}=0.1um, Si substrate	MIT	B. Lu et al., EDL 2010

optimized the GaN/SiO_2 interface using a PECVD oxide followed with a high-temperature (1000°C) nitrogen annealing. We first characterize the MOS capacitors and found the extracted interface state densities to be very low and approaching that in Si MOS [21]. Subsequently, we have, using this GaN MOS process, experimentally demonstrated a record high field-effect inversion electron mobility of 167cm^2/V-s in GaN MOSFETs with ion-implanted source/drain regions. In addition, since then, we have demonstrated several high-voltage enhancement-mode GaN lateral power MOS-gated FET structures (MOSFETs and MOSC-HEMTs) on sapphire substrates [7,15,22-25]. These prototype transistors have specific on-resistances up to more than 50X better than the silicon counterparts at the same blocking voltage range (600-2.5kV) and off-state leakage current density more than 100X less than that in conventional HEMTs. The main advantages of the MOSC-HEMT is the low off-state leakage and low gate leakage current, often several orders of magnitude less than that of conventional HEMTs. On the other hand, the poorer channel mobility in the MOS channel requires the downscaling of the channel length, down to submicron dimensions, to

minimize the dominance of the channel on-resistance [24,26].

The output I-V characteristics of a 3μm GaN MOSC-HEMT on sapphire substrate with specific on-resistance of 20mΩ-cm^2 are shown in Fig. 5 [23]. We have recently demonstrated a 0.3μm channel GaN MOSC-HEMT on silicon substrate with specific on-resistance of 4mΩ-cm^2 and a breakdown voltage over 350V [24]. Hence, the on-state performance of the HEMT and MOSC-HEMT is now quite similar. In addition, we have found that under avalanche conditions, the MOSC-HEMT is survivable [24] when the drain current is limited but we have not found a report that a HEMT or MOS-HEMT has survived such an avalanche test.

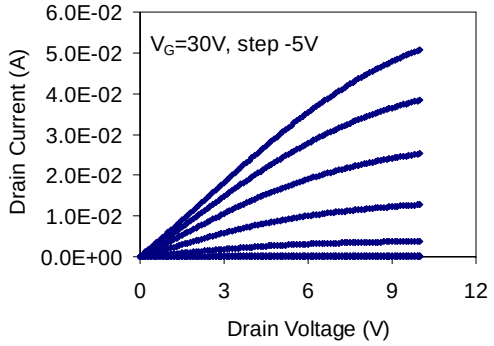


Fig. 5: Output I-V characteristics of GaN MOSC-HEMT with 3μm channel length and 20μm RESURF length

4. TECHNICAL CHALLENGES AND RELIABILITY

The key technical challenges for GaN power FET development and commercialization include current collapse, avalanche capabilities, device ruggedness, threshold voltage control and long-term reliability.

Drain current collapse under ac frequencies is a well-known phenomenon and there are probably many causes. Minimization of surface electric field with field plates and reduced polarization charges are among the many ways to control it (see for example, [24,27]). We would like to point out that our GaN MOS-gated FETs do not exhibit, while MOSC-HEMTs do exhibit, the current collapse behavior commonly seen in AlGaN/GaN HEMTs at room temperature. The temperature dependence of the current collapse behavior is also quite different, indicating the complexities of this degradation phenomenon [28]. Many ways have been suggested to control or increase the threshold voltage control in either MOS-HEMT or MOSC-HEMT (see for example [27]) but more efforts are needed to make it as controllable as that in state-of-art Si nanometer MOSFETs.

4. SUMMARY

We have reviewed the recent advances of high-voltage lateral GaN power FETs. Its successful commercialization will impact many consumer and industrial power electronic applications, resulting in significant energy efficiency and conservation efforts.

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NORMALLY-OFF MODE ALGAN/GAN HEMTS WITH P-INGAN CAP LAYER

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ABSTRACT

In order to realize normally-off HEMTs, which are important for applying them to the high-power switching systems, we proposed to introduce a thin i-InGaN cap layer on a conventional AlGaN/GaN HEMT structure. Polarization-induced field in the InGaN cap layer raises the conduction band of the AlGaN/GaN interface leading to threshold voltage shift to the positive direction. Mg doping in the InGaN cap layer was demonstrate to be effective in shifting the threshold voltage furthermore. Normally-off HEMT with a threshold voltage of 1.2 V and a maximum transconductance of 146 mS/mm was obtained

1. INTRODUCTION

AlGaN/GaN HEMTs receive much attention for high-power and high-frequency applications. In order to apply them to the high-power fail-safe switching systems, normally-off HEMTs are indispensable [1)]. The conventional normally-off HEMTs require a precise etching control for recess gate [2)] or heavy p^+-doping for junction gate [3)]. Previously, we proposed to introduce a thin i-InGaN cap layer on a conventional AlGaN/GaN HEMT structure to implement the normally-off HEMTs [4)]. Polarization-induced field in the InGaN cap layer raises the conduction band of the AlGaN/GaN interface leading to threshold voltage shift to the positive direction.

In this report, we have studied the effect of p-type Mg doping in the InGaN cap layer and succeeded in realizing high-performance normally-off HEMTs.

2. EXPERIMENTAL RESULTS

Fig. 1 shows the schematic cross section of the devices fabricated using p-$In_{0.23}Ga_{0.77}N$ (1×10^{20} cm^{-3}, 4 nm)/i-$Al_{0.21}Ga_{0.79}N$ (17 nm)/i-GaN (2 μm) heterostructure grown by MOCVD on a sapphire substrate. For comparison, control devices without InGaN cap and with i-InGaN cap were also fabricated. The nominal gate length of the devices was 1.5 μm.

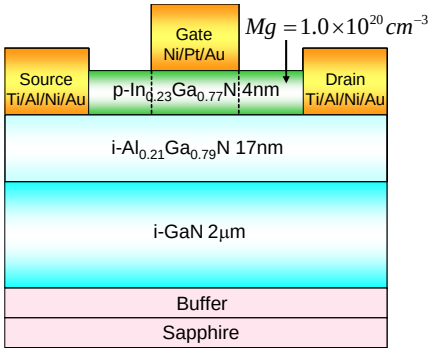

Fig.1 Schematic cross section of the AlGaN/GaN HEMTs with p-InGaN cap layer.

Fig. 2 (a), (b) and (c) show the energy band diagrams of the devices without InGaN cap, with i-InGaN cap and with p-InGaN cap, respectively. For the device without InGaN cap, 2DEG will be formed at the interface of AlGaN/GaN layers even with no positive gate bias due to the polarization charge, as shown in Fig.2 (a). Meanwhile, for the device with i-InGaN cap, the conduction band is raised as shown in Fig.2 (b), resulting in a normally-off operation of the device. For the device with p-InGaN cap, the conduction band is raised further due to p-doping in the InGaN cap layer as shown in Fig.2 (c). Then, it is expected that the threshold voltage of the device will shift further toward the positive direction.

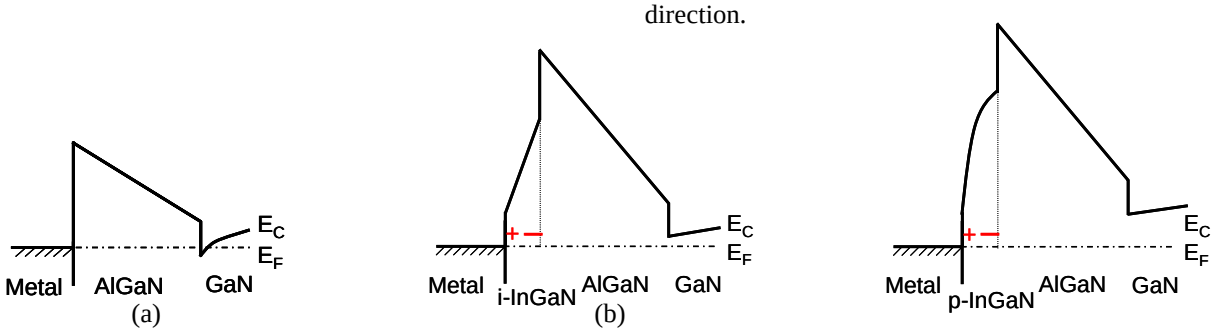

Fig.2 Energy band diagrams of the AlGaN/GaN HEMTs (a) without InGaN cap, (b) with i-InGaN cap (c) with p-InGaN cap, respectively.

Fig. 3 shows the dependence of I_D-V_{GS} characteristics of the AlGaN/GaN HEMTs with p-InGaN cap on the temperature of Mg-activation annealing. The annealing was performed for 20 minutes in N_2 ambient. As shown in Fig.3, the largest shift of the threshold voltage was obtained for the device annealed at 800°C.

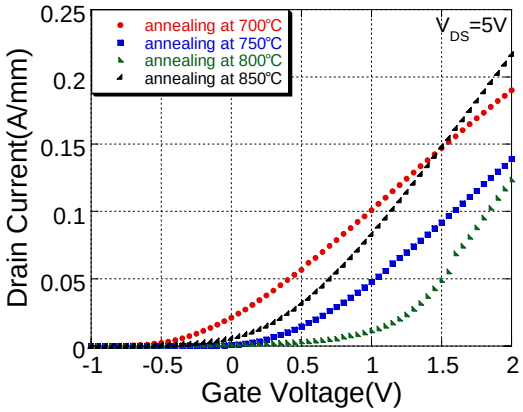

Fig.3 Dependence of transfer characteristics of the AlGaN/GaN HEMTs with p-InGaN cap layer on annealing temperature.

Fig. 4 (a) shows the comparison of I_D-V_{GS} characteristics of the devices without InGaN cap, with i-InGaN cap and with p-InGaN cap, respectively, annealed at 800°C. As expected, compared to the device without InGaN cap, the threshold voltage of the device with i-InGaN cap shifted toward the positive direction, and the threshold voltage of the device with p-InGaN cap shifted further. The threshold voltages evaluated by extrapolating the drain current to zero were -1.0 V, -0.2 V and 1.2 V for the AlGaN/GaN HEMTs without InGaN cap, with i-InGaN cap and with p-InGaN cap, respectively.

Fig. 4 (b) shows the comparison of g_m-V_{GS} characteristics of the devices without InGaN cap, with i-InGaN cap and with p-InGaN cap annealed at 800°C, respectively. Highest g_{mmax} of 146 mS/mm was obtained for the device with p-InGaN cap, as shown in the figure.

3. CONCLUSION

In conclusion, AlGaN/GaN HEMTs with p-$In_{0.23}Ga_{0.77}N$ cap layer were successfully fabricated. It has been demonstrated that the introduction of p-InGaN cap layer was effective in shifting the threshold voltage toward the positive direction and realizing normally-off HEMTs.

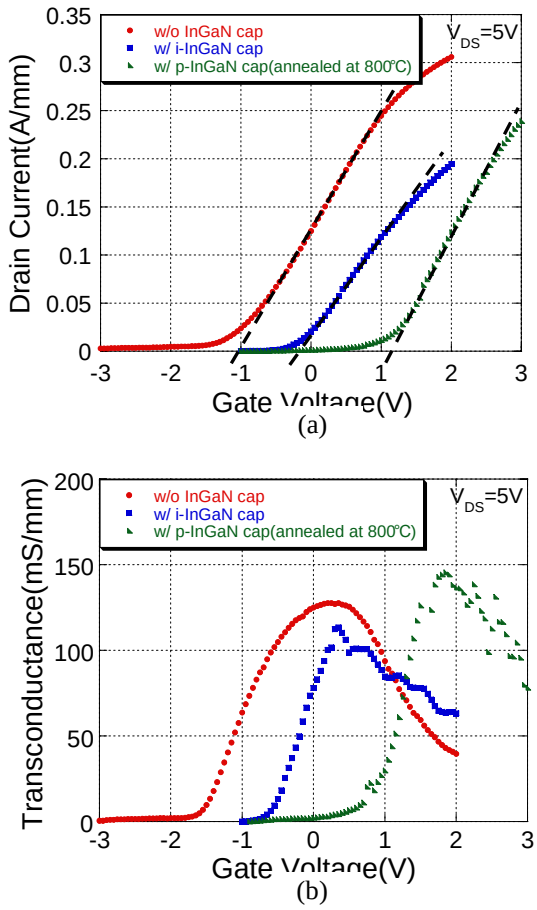

Fig.4 Comparison of transfer characteristics of the AlGaN/GaN HEMTs without InGaN cap, with i-InGaN cap and with p-InGaN cap annealed at 800°C, respectively.

ACKNOWLEDGEMENTS

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HIGH VOLTAGE POWER TRANSISTOR DESIGN – INFLUENCE OF METALLIC CONTACT AREA ON DEVICE BREAKDOWN

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ABSTRACT

Our work studies the impact of ohmic and Schottky contact area scaling on vertical through buffer breakdown voltage. A correlation between increase of metal contact area on active semiconductor region and early breakdown probability has been observed. Additionally we discuss design rules for high breakdown devices.

1. INTRODUCTION

Large area GaN power transistors on conductive *n*-type SiC substrates for current levels of several tenths of amperes and breakdown voltages up to 1000 V require a careful optimization of all metallizations directly contacting the semiconductor surface. Vertical defects in the epitaxial GaN buffer layer may lead to early breakdown effects if a leakage path from the topside contact to the conductive substrate is provided [1]. Since ohmic and Schottky contacts cover a significant fraction of the active transistor area this becomes a matter of concern for large scale devices. It is therefore straight forward to investigate the influence of metal contact areal distribution on vertical breakdown voltage.

2. FABRICATION AND CHARACTERISATION

HEMT epitaxial structures are grown by MOCVD (metal-organic chemical vapor deposition) on n-type SiC substrates. The epitaxial structure of wafers A and B consists of AlN nucleation layer, 3 µm GaN:C buffer, 100 nm uid GaN channel, 13 nm AlGaN barrier and 3 nm nid GaN cap. The structure of both wafers is similar excepting difference of growth conditions of AlN layer.
For characterization of vertical breakdown test structures consist of circular ohmic/Schottky metal pads with diameters of 80 (size 1), 150 (size 2) and 300 (size 3) µm are used. Contact areas are 5×10^{-3}, 17×10^{-3} and 70×10^{-3} mm², respectively. The Ti/Al/Mo/Au-based ohmic contacts are produced by e-beam evaporation and annealed at 830 °C. The Schottky contacts are fabricated by e-beam evaporation of Ir/Ti/Au. Contact pads are laterally isolated by $^{14}N^{+}$ ion implantation. Additionally some Schottky contacts are fabricated on implanted region. Vertical breakdown is measured by increasing of positive/negative voltage on contact pad in 2 V steps while wafer backside is grounded. As failure condition an absolute current limit of 1 mA is used.

3. RESULTS AND DISCUSSION

Fig. 1 shows area normalized *I-V* curves of vertical breakdown measurements in positive and negative direction on ohmic contacts.

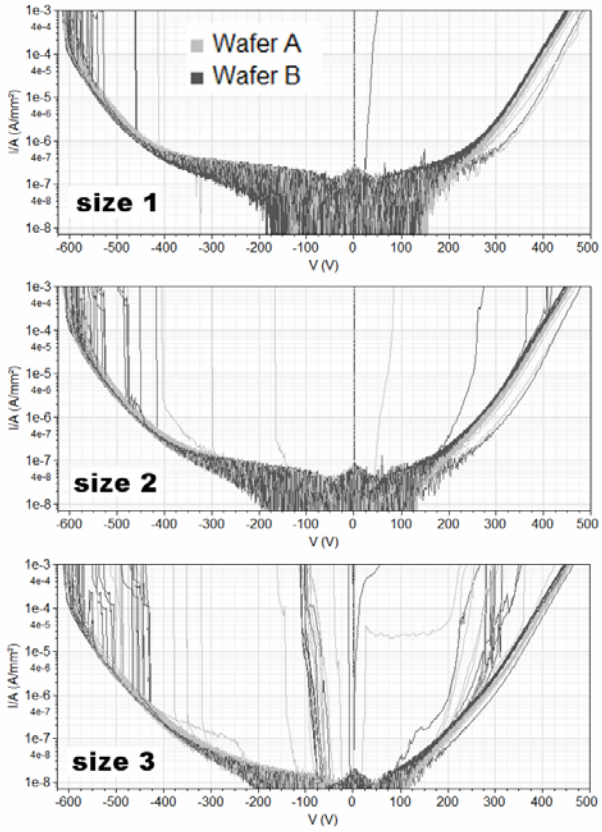

Fig.1: Area normalized *I-V* curves on ohmic contacts in both positive and negative direction sorted by size.

At a first glance it could be seen that there is no difference between wafers A and B. For all sizes area specific current per area I/A increases non linearly with voltage.
In positive direction most test structures of size 1 and 2 follow this curve with low range of variation until the absolute current limitation of 1×10^{-4} A is achieved. This corresponds to breakdown voltage of above 450 V. For size 3 significant amounts of structures shows earlier current increase at voltages above 250 V. After breakdown tests most of the structures do not show any visible material degradation, similarly measurement repetitions do not lead to significant changes.

In negative direction *I-V* characteristics show similar behavior. However, current increase starts at higher bias with shift of about 150 V. At higher voltages "hard" breakdown is dominant – the current rise up very fast and arcing occurs. Such kind of breakdown leads to visible material destruction. Additionally, for largest contact area other breakdown mechanism becomes visible. It shows after small shift of about 50 V near linear rapid current increase within range of 100 V.
Since Mo-based ohmic contacts are know for spikes building during formation [2], comparison between ohmic contacts and Schottky contacts on implanted and non-implanted areas has also been done. Fig. 2 shows area normalized *I-V* curves for all contact types on size 3 structures.

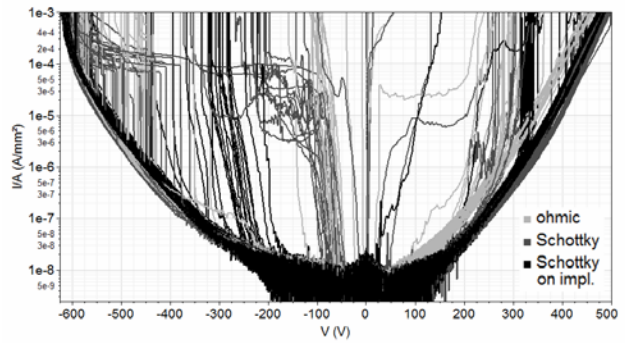

Fig.2: Area normalized *I-V* curves on ohmic contacts and Schottky contacts on non implanted and implanted areas on size 3.

Obviously all contact types show the same non linear *I-V* behavior. Additionally, in negative bias direction both, ohmic and Schottky contacts on active areas show "early" breakdown events at bias voltages below 100 V. However, for Schottky contacts on implanted area such "early" breakdown typically starts at higher voltages above 250 V. More detailed information on this issue is given in Fig. 3. Since some Schottky contact structures show first current increase which then stabilize at about 1×10^{-4} A/mm², current limit for histogram has been set to I/A=1×10^{-5} A/mm².

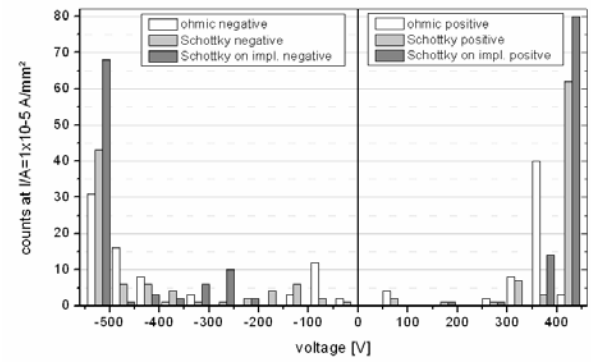

Fig.3: Histogram of breakdown voltages for size 3 ohmic and Schottky contacts at I/A=1×10^{-5} A/mm² condition.

There are two count peaks for early breakthrough in negative direction: One peak at around 100 V for ohmic/Schottky contacts on active region and at above 250 V on implanted region.

Since the "early" vertical breakdown mechanisms seem to be similar for ohmic and Schottky contacts on active region we assume that ohmic contact spiking plays minor role only. Whereas current transport through extended epitaxial defects such as screw and edge dislocations could be a possible explanation. Isolation implantation underneath the Schottky metal additionally contact creates a high resistive region of approximately 100-300 nm thickness. This is responsible for the observed breakdown shifting of 150 V to the more negative side.

4. CONCLUSIONS

In our study we compared the influence of metal contact area scaling and different contact types on vertical breakdown. We demonstrated that increase of metal contact area on active device region is combined with higher risk of early breakdown.
Based on the presented data we derived device dimensions which would allow statistically reliable breakdown performance up to 600 V. Related to entire area of all measured structures (size 3) 2.5 breakdown events within range of +/- 300 V per mm² active device area have to be taken into account. This significantly reduces maximum transistor size that can be fabricated with high yield. Thus, one of the design rules is to minimize the metalized active device area as far as possible. One possibility is to reduce ohmic contact and pad areas to geometries that are absolutely necessary for device performance.

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AlGaN/GaN/GaN:C BACK-BARRIER SCHOTTKY DIODES FOR POWER SWITCHING

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ABSTRACT

A GaN-based heterostructure lateral Schottky diode with insulating carbon-doped GaN back-barrier with high reverse bias blocking capability for high voltage operation in power switching is presented. The device combines the low onset voltage, 0.46 V, of a recessed Schottky contact with low leakage current at reverse bias and the good blocking capability of a GaN:C back-barrier. Devices with a 15 µm anode cathode separation exhibit leakage current as low as 6×10^{-6} A, reverse blocking bias over 1000 V and on-state resistance of 1.48 mΩ × cm^2.

1. INTRODUCTION

Conduction losses in the ON-state, onset voltage and reverse bias leakage give significant limitations to the power-switch performance of Schottky diodes. GaN-based heterostructure Schottky diodes owning properties of high sheet-carrier density and high mobility in the two dimensional electron gas (2DEG) channel and large breakdown field-strength, showed superior performance for high-power switching applications [1] in terms of low conduction losses and also low switching losses. The high blocking capability of these devices is linked to the high bandgap of 3.4 eV of GaN. However, most wide bandgap material Schottky-diodes show an undisired high onset voltage with the associated losses in on-state operation. Here we demonstrate an efficient and robust way to reduce the onset voltage in GaN based lateral diodes without sacrifycing neither the on-state resistance nor the blocking voltage.

GaN based-HEMTs with integrated serial recessed Schottky protection diode have already been demonstrated [2], owning low onset voltage and high reverse bias blocking capability along with good large signal microwave performance. The Schottky diode contacts very good to the 2DEG in a HFET structure. The use of GaN:C back-barrier in GaN-based HEMT devices has already demonstrated the ability to suppress the reverse bias leakage of Schottky contacts and enhance the devices' breakdown voltage [3], [4]. Here we present for the first time integration of GaN-based lateral diode with a recessed anode topography with GaN:C back-barrier for the use in power-switching electronics.

2. EXPERIMENTAL SET AND RESULTS

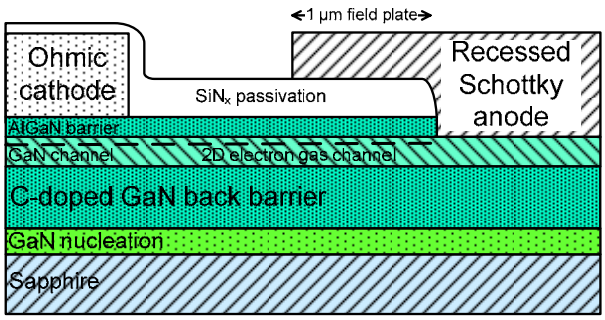

Fig. 1: Schematic sketch of the fully recessed Schottky diode with GaN:C back-barrier.

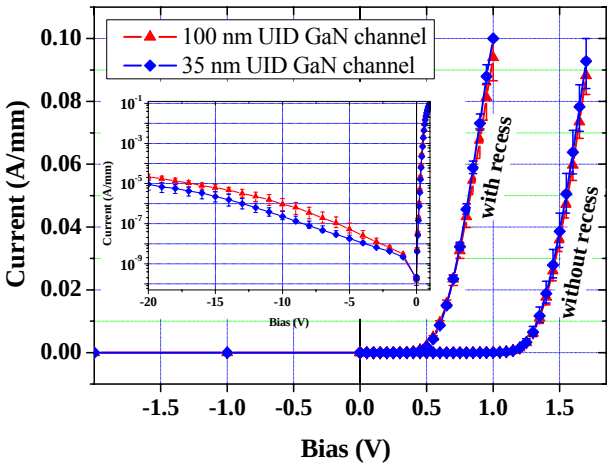

Fig. 2: Wafer level median diode characteristics of devices (W = 100 µm and L_{AC} = 2 µm) with GaN:C back-barrier with two different UID GaN channel thicknesses (error bars are 25% and 75% percentiles). (inset) Log scale of the reverse bias regime.

The samples are grown by MOVPE on sapphire wafers owning a ~25 nm GaN seeding layer followed by a 1.5 µm carbon doped buffer layer, (GaN:C, ~1×10^{17} cm^{-3} measured by SIMS). The active layers grown on top of the buffer consist of UID GaN channel followed by 24 nm $Al_{0.22}GaN$ barrier layer. For comparison two types of samples were grown, i.e. UID GaN channel thickness, d_{Ch}, of 35 nm (Wafer "A") and 100 nm (Wafer "B"), were examined. Schottky diodes were fabricated on both wafers types. Ti/Al/Mo/Au based cathode ohmic contacts were evaporated and annealed at 830°C. Inter device isolation was made using $^{14}N^+$ multi energy implantation. The AlGaN barrier was passivated with 150 nm SiN_x. A trench in the passivation for the anode Schottky contacts

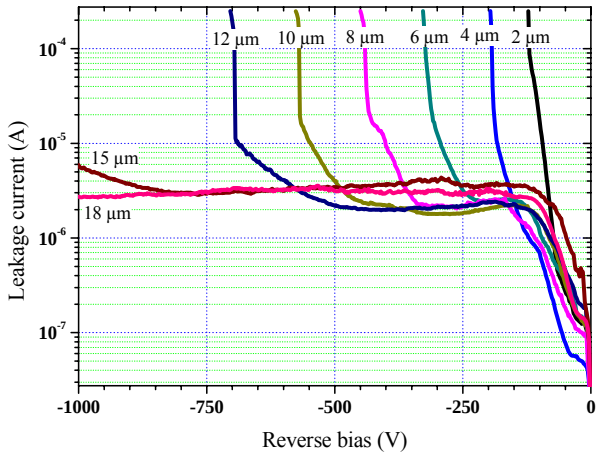

Fig. 3: Diodes'(Wafer "B") reverse bias current output measurements for devices with different anode-cathode separation L_{AC} and $W = 2 \times 125$ µm. The measurement is limited by the current compliance of 1 mA/mm and drain bias $V_{DS} = 1000$ V.

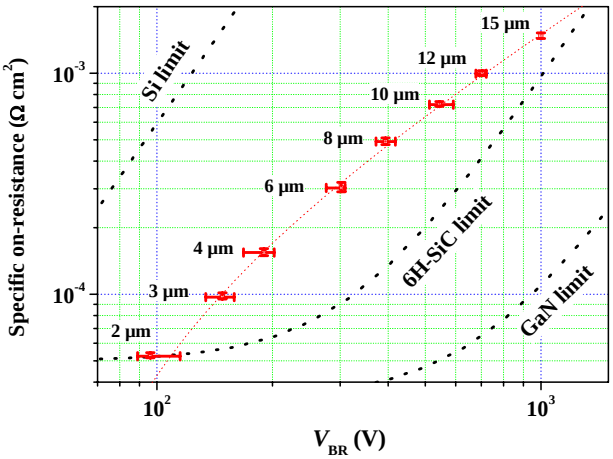

Fig. 4: Wafer level (Wafer "B") median diode V_{BR} vs. $R_{ON} \times A$ for $W = 250$ µm and $L_{AC} = 2$ µm to 15 µm devices (error bars are 25% and 75% percentiles). Dotted connecting line is a quadratic fit.

was defined by lithography and subsequently etched. The AlGaN layer in the opened trench was fully recessed by BCl_3 based reactive ion etching using the same lithographic mask. The recess etch depth was estimated as 35 nm. Pt/Ti/Au contacts were then evaporated for the anode Schottky metal, followed by a metal lift off. The fabricated devices were 250 µm wide with anode-cathode separation, L_{AC}, of 2 µm to 15 µm with 1 µm overlapping field plate. A cross section of the devices is illustrated in Fig. 1.

Fig. 2 shows the wafer level median diode forward and reverse characteristics for the different wafers type. It could be seen that the significance of the UID GaN channel thickness has a minor influence on the diode DC performance. Comparison of recessed-anode diodes to planar diodes on the same wafer show significant reduction of the diode onset voltage from 1.2 V to about 0.46 V at 1 mA/mm independent of anode-cathode separation and of the UID GaN channel thickness.

The devices' ON-state resistance was calculated as $5.2 \times 10^{-5}\ \Omega \cdot cm^2$ and $1.5 \times 10^{-3}\ \Omega \cdot cm^2$ and the diodes' maximum forward current, I_{max}, between 0.9 mA/mm and 0.4 mA/mm for L_{AC} of 2 µm and 15 µm respectively.

The diodes' reverse bias characteristics displayed in Fig. 2 inset indicate weak reduction of the Schottky contact reverse bias leakage for devices owning $d_{Ch} = 35$ nm compared to the wider channel.

The diodes reverse bias characteristics of devices with anode-cathode separation, $L_{AC} = 2$ µm to 18 µm is presented in Fig. 3. Devices with $L_{AC} \geq 15$ µm exceed reverse blocking bias of 1000 V. A strong dependence of the diodes reverse bias blocking capability on the anode-cathode separation is observed. In addition saturation of the reverse leakage current at $\sim 1.5 \times 10^{-6}$ A is observed.

The wafer level (Wafer "B") ON-state resistance versus the reverse maximum blocking bias characteristics is shown in Fig. 4. A quadratic dependence of the reverse blocking bias on the diode separation, L_{AC}, is observed.

3. CONCLUSIONS

GaN-based lateral Schottky diodes with GaN:C back-barrier and with complete recessed AlGaN barrier were demonstrated. The recessed anode showed a superior Schottky contact to the GaN channel [2] with significant reduction of the diode onset voltage but without impact on the ON-state resistance and the forward bias current.

The use of GaN:C back-barrier reduced the Schottky reverse bias leakage and enabled the diodes high blocking voltage and a quadratic scale with the diode geometry. Insignificant influence of the UID GaN channel thickness on the devices' dc characteristics was observed.

The diodes showed robust process capability with state of the art performance.

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PROGRESSES IN GaN POWER RECTIFIER

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ABSTRACT

In this work, we demonstrate that high quality Schottky diodes can be obtained on GaN heteroepitaxially grown on sapphire by MOCVD. Ni and Ti/Al were used to obtain respectively Schottky and Ohmic contacts using RTA annealings. Adequate passivation steps and insertion of a resistive guard ring were also implemented. Finally, ideality factors of 1,07 as well as a barrier height of 1,06 eV were obtained on pv-SBD devices that have a breakdown voltage over 600V.

1. INTRODUCTION

Power microelectronics tries continuously to improve device performances and hence, has to face new challenges. The realization of fast switching and rectifying devices able to match the increase of switching frequency is one of them. In this context, silicon probably reaches its limits while wide band gap materials seem to be attractive. For more than two decades, silicon carbide (SiC) has been intensively studied and 4H-SiC rectifiers are now commercially available from at least 3 industrial sources. Nevertheless, the substrate quality, dimension and availability, that strongly impact the die cost, limit their developments. For such reasons, other semiconductors, particularly III-N compounds, are now more and more under studies [1]. Among them, gallium nitride (GaN), with its wide band gap, high electrical critical field and high saturation velocity (even higher than for SiC) seems to be an excellent candidate for power devices with higher performances in terms of current density or reverse breakdown voltage. Extensive efforts have been made to achieve high-quality GaN layer grown by heteroepitaxy on sapphire and silicon wafers, leading to structures now compatible with rectifying devices at more reasonable cost. If an abundant literature can be found on both ohmic and rectifying contacts, central parts of the Schottky devices, few papers present complete structures and their performances. Companies such as Velox, MicroGaN or Azzurro have already demonstrated the possibility to achieve 600V GaN Schottky diodes. Nevertheless, the devices are not yet commercially available.

In this paper, we will review all the requested steps to achieve a high quality GaN power rectifier. We will present the results we have obtained for complete structure and compare them with the one previously cited.

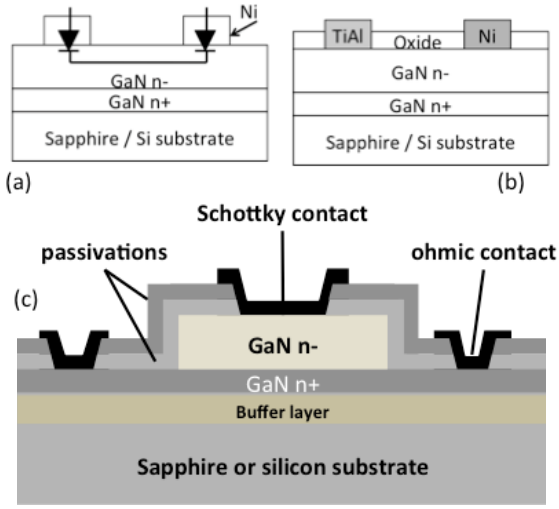

Fig. 1: Description of the STS (a), l-SBD (b) and pv-SBD (c) realized structures.

2. EXPERIMENTS

In this work, a low doped n-type GaN on a high doped n-type GaN has been epitaxially grown by MOCVD (Metal-Organic Chemical-Vapor-Deposition) using a buffer layer on both Si (G2REC epitaxial group, [2]) and sapphire (Velox). Authors want to mention, at this point, that layer thicknesses and buffer layers are specific to wafer materials. For this study, different structures were carried out. Ohmic contact was evaluated through classical c-TLM structure. Then, as presented on Fig. 1a, a "Schottky To Schottky" structure (STS), that allows us to access the leakage current with a maximum of two photolithography steps and a wet etching process, will be reviewed. Both lateral Schottky Barrier Diode (l-SBD) realized on the low doped GaN layer, as depicted in Fig. 1.b, and pseudo-vertical (pv) -SBD have been processed (Fig. 1.c) and then electrically characterized using an automatic probe station. For these structures, ohmic contacts have been prepared using Ti/Al deposited by PVD and then RTA annealed at 650°C during 3min. Such conditions lead to specific contact resistance around $1x10^{-5}\Omega.cm^2$ [3]. The Schottky contacts consist in a PVD Ni layer annealed under Ar at 450°C [4]. The electrical

measurements were then performed in temperature from ambient to 125°C using kelvin probes.

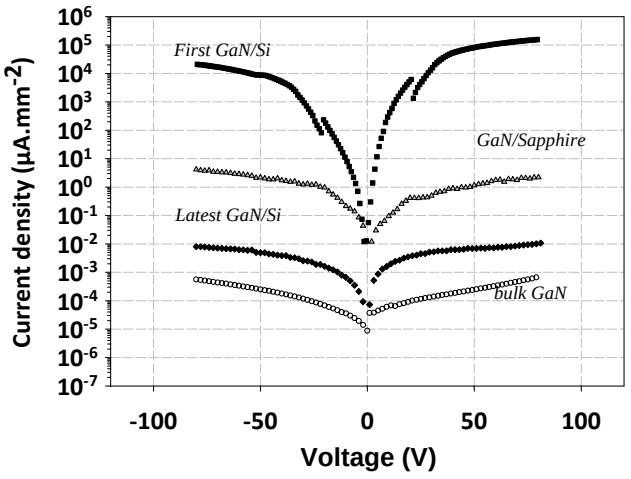

Fig. 2: STS structure I-V characterizations for different hetero-epitaxial materials

3. RESULTS AND DISCUSSION

First, "Schottky to Schottky" structures (STS) were realized through standard photolithography process. It allows us to study the reverse leakage current depending on process parameters such as Schottky layer thickness, contact annealing temperature or duration and presence of an insulation step and to simply discriminate various process parameters with only two masking levels. This has allowed us to define a valuable Schottky contact, done in this study by a Ni layer annealed using RTA process at 450°C. Moreover, STS may help to discriminate the epitaxial material quality, giving a kind of "figure of merit" for them. In Fig. 2, one can see a comparison of current density versus voltage (J-V) characteristics for different GaN epitaxial materials. First, bulk GaN material remains a reference case with the lowest J values, with around 3 orders of magnitude compared to GaN on sapphire. In this figure, one can also see the progresses that have been done on GaN grown on Si giving even better results than the one on sapphire. This is an encouraging result visualizing progresses done on Si wafers and the one that still need to be done.

Then, Schottky Barrier Diodes (SBD) with Ni and Ti/Al, respectively for Schottky and ohmic contacts, were realized. Ti(50nm)/Al(200nm) bi-layer contacts were sputtered and annealed at 650°C during 60s [3]. Diodes were patterned through standard photolithography processes. An adequate insulation step was implemented in the structure as well as a resistive guard ring, realized by Mg implantations without any further annealing. The electrical measurements were then performed for temperatures ranging from ambient to 125°C. Using the classical J-V plots, as the one presented on Fig.3, breakdown voltage (Reverse) as well as barrier heights and ideality factors (forward) have been extracted.
The breakdown voltages obtained in our study were always measured over 600V whatever is the temperature of electrical characterisation. This is an interesting result corresponding to the expectations for such devices. When extracting the ideality factor, we have found that n is extremely stable in temperature (n=1,07±0,03) confirming the device quality. Finally, using a

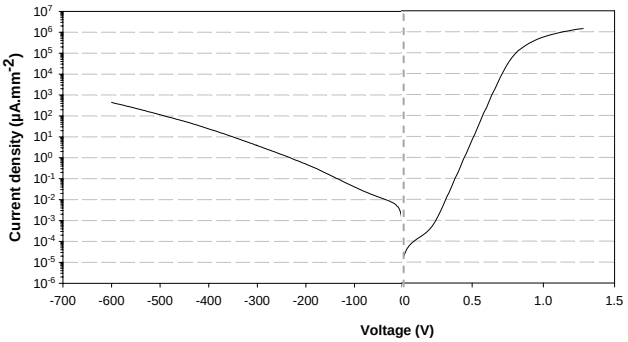

Fig. 3: Reverse and forward current density-voltage characteristics for a Ni based pv-SBD

Richardson plot, barrier height was found to be Φ_B=1.06eV which is one of the best values published in the literature. This work evidences that good devices may be achieved on GaN hetero-epitaxially grown on sapphire or silicon when using a pv-SBD structure including a resistive guard ring around the Schottky contact.

4. CONCLUSION

In this work, we have shown that STS structures are interesting to discriminate between different hetero-epitaxial materials. Concerning the pv-SBD realized here, a high barrier height (Φ_B=1.06eV) with a low ideality factor (n=1.07) and a breakdown value (V_{BR}) largely over the expected value of 600V were found, leading to one of the best "up to date" results in the literature. Nevertheless, efforts must be done continuously to decrease the leakage current and increase device reliability.

ACKNOWLEDGMENTS

The authors would like to thank CRHEA-CNRS, OMMIC and Picogiga (G2REC epitaxial group) for their constant efforts to provide MOCVD GaN grown on Si wafers as well as Velox Semiconductor Corporation for GaN on Sapphire. We would also like to thank Pr. C. Brylinski at LMI (Lyon) for valuable discussions. This work was financially supported by the OSEO project G2REC

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IMPACT OF SURFACE PROCESSING ON THE ELECTRICAL PROPERTIES OF P-TYPE IMPLANTED 4H-SiC FOR POWER DEVICES

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ABSTRACT

In this paper, the influence of the morphology of Al-implanted silicon carbide (4H-SiC), annealed *with* and *without* a carbon capping layer, on the microstructure and electrical properties of alloyed Ti/Al Ohmic contacts, is discussed. The improved SiC morphology, obtained using a capping layer during annealing, resulted in a reduction of the roughness (from 44 nm to 23 nm) and of specific contact resistance ρ_c (~ 10^{-4} Ωcm^2) of the contacts. From the temperature dependence of ρ_c a Schottky barrier height Φ_B in the range 0.46-0.51 eV was determined and correlated to the interfacial structure. Preliminary results showed that the morphology of p-type implanted SiC can impact also the electrical parameters of MOSFETs.

1. INTRODUCTION

Due to its outstanding physical properties, silicon carbide (SiC) is the material of choice for the next generation of power electronic devices [1]. In power devices, good Ohmic contacts with a low specific contact resistance (ρ_c) are required to decrease the power dissipation. However, the fabrication of low-resistance Ohmic contacts is difficult, because of the high metal/p-SiC Schottky barriers and the high ionization energies of p-type dopants. Furthermore, the thermal budget for the electrical activation of p-type dopants (up to 1800°C) can induce a significant surface roughness in SiC [2]. This effect can be mitigated by protecting the surface with a carbon capping layer during annealing [3,4].

In this paper, the influence of a different morphology of Al-implanted SiC, resulting from different annealing conditions, on the electrical and structural properties of alloyed Ti/Al Ohmic contacts is discussed. As an example, it will be also briefly shown how the different surface morphology of p-type implanted SiC can impact important electrical parameters of 4H-SiC MOSFETs.

2. EXPERIMENTS

N-type 4H-SiC epitaxial layers (with $N_D=1.0\times10^{16}$ cm^{-3}), 6μm-thick, grown on heavily doped n^+-type substrate, were used. Al^+-implantation at different energies (30-80 keV) and at a dose of 1.3×10^{15} cm^{-2} was performed to create an almost uniform p-type dopant profile. Post-implantation annealing at 1700 °C was carried out for electrical activation of the dopant, *with* and *without* a protective carbon capping layer. The metal contacts on the p-type Al^+-implanted regions were formed by a Ti/Al bilayer annealed at 950°C. The specific contact resistance was determined using transmission line model (TLM) structures. The morphology and the microstructure of the contacts were investigated by atomic force microscopy (AFM) and X-ray diffraction (XRD).

3. RESULTS AND DISCUSSION

The morphology of SiC implanted regions and Ti/Al Ohmic contacts was monitored by AFM. After post-implantation annealing, AFM analysis showed a large roughness (RMS=18.9 nm) in the samples annealed at 1700°C *without* the protective carbon capping layer, while a significant lower RMS (2.4 nm) was measured in the samples annealed *with* the capping layer. On the other hand, the morphology of alloyed Ti/Al contacts formed on these surfaces was affected by the large RMS of the underlying SiC. In fact, the RMS values measured of the contacts were 44.0 nm and 22.8 nm, for the SiC substrate annealed *without* and *with* the use of capping layer, respectively. These results are summarized in Table 1.

	Without Cap	**With Cap**
RMS of implanted and annealed (1700°C) 4H–SiC	18.9 nm	2.4 nm
RMS of alloyed Ti/Al contacts	44.0 nm	22.8 nm

Table 1: Surface roughness (RMS) of implanted and annealed 4H-SiC and alloyed Ti/Al contacts, for different annealing conditions.

The alloyed Ti/Al Ohmic contacts also showed a different electrical behaviour, depending on whether the capping layer was used or not. The results of TLM measurements, performed at room temperature, are reported in Table 2. In particular, Ti/Al contacts formed on the capped sample exhibit a lower specific contact resistance (1.45×10^{-4} Ωcm^2) than to those formed on the uncapped sample, (3.51×10^{-4} Ωcm^2). This improvement was even much pronounced at a lower Al-implantation dose. It must be pointed out that alloyed Ti/Al contacts enabled an improvement of ρ_c with respect to nickel silicide (Ni_2Si) contacts. In this latter case, almost no dependence of ρ_c on the use of a capping layer (ρ_c ~ 4.5-6 $\times10^{-2}$ Ωcm^2) was

observed, since the formation of Ni_2Si is associated to the consumption of part of the SiC surface [5].

	Without Cap	With Cap
ρ_c of Ti/Al	$1.45\times10^{-4}\,\Omega cm^2$	$3.51\times10^{-4}\,\Omega cm^2$
ρ_c of Ni_2Si	$6.01\times10^{-2}\,\Omega cm^2$	$4.50\times10^{-2}\,\Omega cm^2$

Table 2: Specific contact resistance ρ_c of alloyed Ti/Al and Ni_2Si contacts to p-type SiC for different annealing conditions.

The XRD pattern, reported in Fig. 1 for the sample *with* capping layer, shows the formation of a ternary compound Ti_3SiC_2, of the Al_3Ti phase, and the presence of unreacted Al. The same features were observed in the samples annealed *without* capping layer. However, transmission electron microscopy analysis (TEM), showed an inhomogeneous interface with a different distribution of the formed phases in the two cases [6].
The current transport at the Al/Ti/SiC interface was studied monitoring the temperature dependence of the specific contact resistance. Fig. 2 shows a plot of ρ_c as a function of the temperature *T*, for the samples annealed *with* and *without* capping layer. In both cases ρ_c decreases with increasing temperatures *T*.

The experimental values of ρ_c were fitted with the thermionic field emission (TFE) model [7].

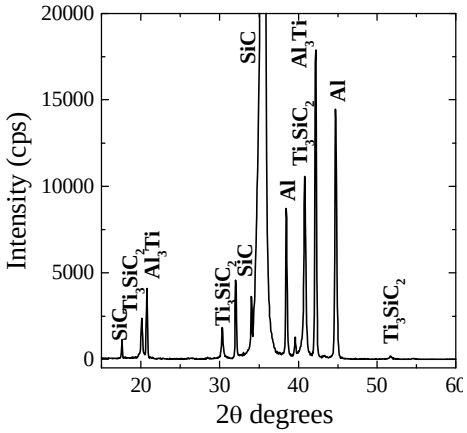

Fig.1: XRD pattern of alloyed Ti/Al contacts for the sample with capping layer.

From the fits of the temperature dependence of ρ_c, the effective barrier height Φ_B could be determined. A reduction of Φ_B from 0.51 to 0.46 eV was measured using the capping layer, that could be correlated with the different interfacial microstructure observed by TEM analysis [6] and is consistent with the reduction of ρ_c.

Preliminary measurements performed in lateral implanted MOSFETs showed that the different surface morphology of the p-type implanted body region can affect fundamental parameters like the channel mobility μ and the threshold-voltage V_{TH}. In particular, a higher threshold voltage and a lower channel mobility were measured in devices subjected to an annealing *with* capping (see summary in Table 3). A higher interface trapped charges density in the devices processed with the capping layer can explain the reduced channel mobility and the increase of V_{TH}.

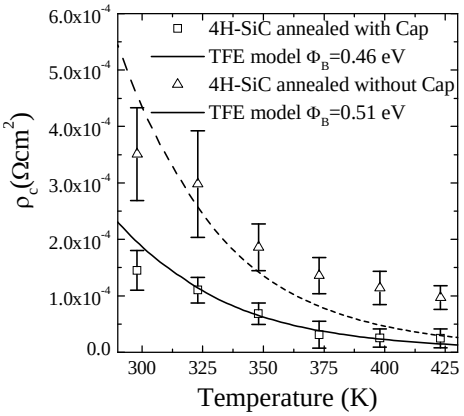

Fig.2: Specific contact resistance versus temperature for alloyed Ti/Al contacts for the samples with and without capping layer.

	Without Cap	With Cap
V_{TH} (V)	6.28	7.15
μ_{FE} ($cm^2V^{-1}s^{-1}$)	38.9	23.5

Table 3: Threshold voltage and channel mobility values for lateral 4H-SiC MOSFETs processed *without* and *with* capping layer.

4. SUMMARY

In summary, it has been shown that the electrical properties of alloyed Ti/Al Ohmic contacts to p-type implanted 4H-SiC can be improved when the contacts are formed on smoother surfaces. The lower specific contact resistance is explained by a lowering of the barrier height. The different surface processing can ultimately impact also the electrical parameters of more complex devices, like MOSFETs.

ACKNOWLEDGEMENTS

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PERFORMANCE AND BIAS TEMPERATURE INSTABILITY CHARACTERISTICS OF 4H-SIC MOSFETS WITH NITRIDED GATE OXIDE GROWN BY RTP

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ABSTRACT

The performance and bias temperature instability (BTI) characteristics of 4H-SiC n-channel MOSFETs with RTP-nitrided gate-oxide are investigated. Relatively high channel mobility is obtained together with low threshold voltage. As well, no significant threshold voltage and drain current shift are observed with respect to constant bias stress both at room and high temperature.

1. INTRODUCTION

SiC power devices have been established as a viable and economical way to improve energy efficiency in the next generation. Promising results have been achieved for 4H-SiC MOSFETs. However, these devices have not yet reached the expected high performance and reliability.
It has been demonstrated that the most effective techniques to improve the MOSFETs performance is the nitridation process. Nevertheless, the threshold voltage stability of MOSFETs with these nitrided gate oxides is influenced by low-field bias, even at room temperature, for both lateral [1] and vertical channels [2, 3]. Bias temperature instability (BTI) is a serious reliability issue and a lifetime limiting factor for the n-channel MOSFETs with these kinds of gate oxides [4]. Previously, we have shown that by using rapid thermal processing (RTP), the oxide growth is two orders of magnitude faster and, the resulting dielectrics exhibit a reduced effective charge and a less defective interface compared to oxides grown by conventional N_2O oxidation.
In this work, we have evaluated the performance and bias temperature instability (BTI) characteristics of 4H-SiC MOSFETs with nitrided gate oxide grown by RTP at high temperature.

2. EXPERIMENT DETAILS

The nMOSFETs have been fabricated on 10 μm p-type epitaxial layers with a doping concentration of 1×10^{16} cm^{-3}, grown 4º off-axis on Si-face of n-type 4H-SiC substrates. The gate oxidation process was performed in a RTP furnace using a silicon wafer as susceptor [5]. Prior to gate oxidation, a surface pre-treatment consisting in an *in-situ* RTA step was carried out in H_2 at 800ºC for 2 min. Then, the rapid thermal oxidation was performed in 100% N_2O at 1050°C for 10 min, resulting in an average oxide thickness of 45 nm. A rapid post-oxidation annealing step was next performed under Ar for 3 min *in-situ* when cooling the system down to 800ºC. Aluminium and nickel were then deposited and patterned to form the gate and source/drain contacts, respectively. The ohmic contacts were annealed at 900 °C in Ar ambient.
The standard bias-stress measurements consist in four different gate biasing steps for each stress time [1]. Initially, the gate voltage is swept from negative to positive bias, at a drain bias of 100 mV, using a Keithley 251 IV SMU. Next, a positive bias is applied to the gate for a given bias-stress time with the other terminals grounded. Then, the gate voltage is ramped from positive to negative bias to determine the shift of the $I_{ds}(V_{gs})$ characteristics. A negative bias equal in magnitude but opposite in polarity is then applied to the gate for the same bias-stress time. Finally, the gate voltage is swept again from negative to positive bias to measure the return shift. The gate bias was interrupted at a fixed time to record the transfer characteristic. The threshold voltage was measured from the $I_{ds}(V_{gs})$ characteristics using the constant current method [1].

3. RESULTS AND DISCUSSION

Fig. 1 shows typical $I_{ds}(V_{gs})$ and $I_{ds}(V_{ds})$ characteristics of 4H-SiC MOSFETs with gate-oxide fabricated by RTP with H_2 surface treatment before N_2O oxidation. It can be seen that MOSFET devices exhibit good electrical characteristics. The $I_{ds}(V_{ds})$ curves show linear and saturation regions, and from the $I_{ds}(V_{gs})$ curves a low threshold voltage of ~ 2.5 V was obtained. The field-effect mobility was extracted from the transfer curves. Relatively high channel mobility was obtained ~20-30 cm^2/V.s which is comparable to the state of the art [4].

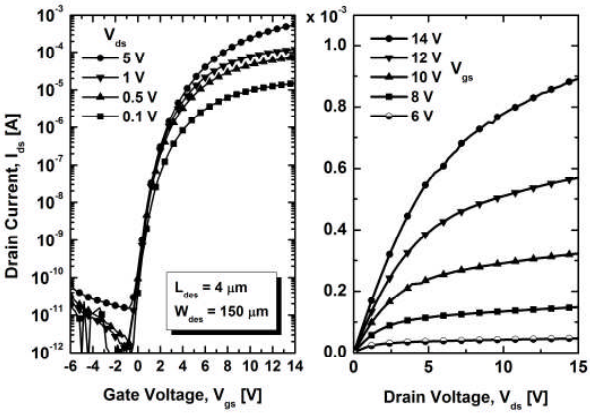

Fig. 1: Electrical characteristics of the investigated MOSFETs (L = 4 μm and W = 150 μm) with H_2 annealing pretreatment and N_2O rapid thermal oxidation.

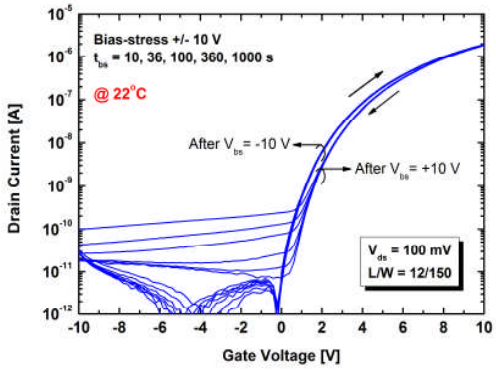

Fig. 2: (a) $I_{ds}(V_{gs})$ characteristics of the 4H-SiC MOSFETs (L = 12 μm and W = 150 μm), as a function of the bias stress time (t_{bs}) at room temperature.

In order to examine the electrical stability of the MOSFET devices with gate oxide grown by RTP, the influence of a prolonged gate bias on the threshold voltage and drain current was investigated for MOSFETs. Fig. 2 illustrates the transfer characteristics' shift for a constant bias stress of ± 10 V at room temperature. The $I_{ds}(V_{gs})$ curves after a positive bias-stress exhibit lower drain currents than those after the corresponding negative bias-stress. A positive bias stress causes a positive shift in the $I_{ds}(V_{gs})$ curves with an almost constant slope; while for a negative bias stress, the curves remain almost unchanged. Moreover, the subthreshold slope of the $I_{ds}(V_{gs})$ curves does not show a large variation during the applied bias stresses, which indicates that the shift may be mainly described in terms of the threshold voltage shift, ΔV_{th}, without mobility degradation. This shows that the creation of electron trapping states at the oxide/SiC interface by the bias stress is negligible and, that the V_{th} degradation is mainly caused by interfacial states generation and electron trapping in the oxide bulk.

Furthermore, the impact of the temperature on the V_{th} degradation was investigated. Positive BTI measurements were performed from 50ºC to 290ºC at a constant bias stress of ± 10 V. Figs. 3(a) and (b) illustrate the instability of the $I_{ds}(V_{gs})$ characteristics as a function of the stress time at 150ºC and 290ºC, respectively. We can observe two different trends when increasing the temperature. Below 150ºC, the $I_{ds}(V_{gs})$ curves exhibit higher drain currents after a positive bias-stress than those after the corresponding negative bias-stress; i.e., a positive bias stress causes a negative shift in the $I_{ds}(V_{gs})$ curves. This is likely due to mobile ions being present [1].

On the contrary, above 150ºC the positive bias-stress causes a positive shift in the $I_{ds}(V_{gs})$ curves. In both cases, the positive bias-stress does not results in a larger variation of the drain current by increasing the bias stress time, and the negative bias-stress restores the drain current close to its initial value. Moreover, it is know that bias-stress can induce leakage current by involving oxide bulk traps for conduction [6]. Both at room and high temperatures, low and stable gate leakage currents were obtained (Fig. 4). This explains the very low drifts of the threshold voltage at high temperature since the creation of electron trapping states by bias-stress is not enhanced.

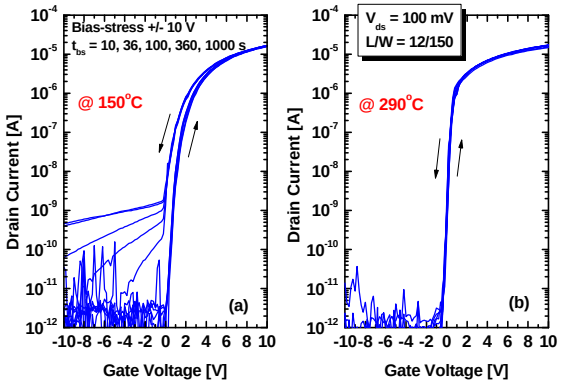

Fig. 3: $I_{ds}(V_{gs})$ curves as a function of the bias stress time (t_{bs}) for a constant bias stress of ± 10 V measured at different temperatures (a) 150ºC and (b) 290ºC.

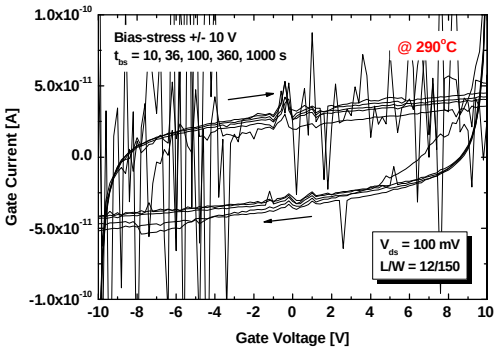

Fig. 4: Typical gate leakage current measured at 290ºC as a function of the bias stress time (t_{bs}) for a constant bias stress of ± 10 V.

4. CONCLUSION

N-channel MOSFETs have been fabricated on 4H-SiC using a gate-oxide process based on oxidation in N_2O by RTP. It has been observed that the performance and bias temperature instability (BTI) characteristics are improved. RTP process has not only the advantage to reduce the thermal budget compared to conventional N_2O oxidation, but also produces MOSFET devices comparable to the state of the art.

ACKNOWLEDGEMENT

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Session 10 :

Optoelectronics, detectors and sensors

Chair : Prof. Joachim Wűrfl

Wednesday June 1, 10:50 - 12:50

AlGaN BASED ARRAYS FOR EXTREME UV DETECTION

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ABSTRACT

Extreme ultraviolet radiations extend from 1 to 200nm. AlGaN alloys offer the opportunity to selectively (versus near UV and visible light) detect them, with a low dark current and a large radiation hardness. MSM detectors and Schottky diodes based on AlGaN heterostructures grown on Si have been fabricated and tested. The spectral responsivity of AlGaN detectors has been measured from 1 to 200 nm in various synchrotron facilities in Europe and our measurements establish the state of the art in the domain. 2D detector arrays (256×256 with a pitch of 10µm; 320×256 with a pitch of 30µm) have been fabricated and hybridized to a Si read out circuit. A prototype camera has been fabricated and has tested. Images in the EUV have been recorded.

1. INTRODUCTION

Extreme ultraviolet (EUV) imaging is crucial in solar observations, as most phenomena on and near the surface of the Sun can be observed in the low wavelength range (1 to 100 nm). On earth, EUV imaging also finds applications in industry, for example for monitoring the beam in the EUV lithography stepper systems or for monotoring the beam in synchrotron facilities.

Wide bandgap semiconductors, such as materials from the aluminum gallium nitride (AlGaN) system can offer significant advantages, provided the technology is mature enough to be considered competitive [1-2]. First of all, AlGaN can have a tunable energy gap, depending on the Al molar fraction, from 3.4 eV up to 6 eV for 0% and 100% Al, respectively. This translates to the cut-off wavelength in the UV range (365 nm down to 200 nm, respectively) and insensitivity to the visible and infrared radiation, reducing the number of filters needed in the system (e.g. a telescope). Furthermore, AlGaN compound is known to be more radiation hard [3-5]. Additionally, due to low leakage currents, AlGaN devices can be operated at room temperature.

AlGaN-based hybrid imagers were demonstrated by several groups [6-9] but they were working on the ultraviolet range only, as they were based on illumination through the sapphire substrate. Fabricating EUV imagers requires a more sophisticated technology. We have chosen an approach based on AlGaN layers grown on Si, front side hybridization to a Si read out circuit, and substrate removal in order to operate the imager in back side illumination [10-14].

2. SINGLE PIXEL DETECTOR

Metal Semiconductor Metal (MSM) and Schottky diodes were fabricated. Pn junctions require p doped layers, which becomes very difficult in Al rich AlGaN layers. As a result, AlGaN pj junctions often include a p:GaN contact layer which severely degrades the spectral selectivity of the detector. Hence, this option was not considered here.

2.1. MSM detectors

MSM do not require any doping and are thus interesting for AlGaN layer with an Al content larger than 50%. However, the detector requires two contacts per pixel which is challenging for small pixels, and require a large bias which may not be compatible with standart Si circuits. Hence, MSM detectors have been tested as single pixel but not considered for arrays. The structures were grown on Si substrates. Various structures were grown. Basically, they all include a thin AlGaN layer (about 300 nm) grown either directly on a very thin AlN buffer or grown on a more complicated structures including AlN and GaN layers. They were mainly measured in the front side side illumination geometry so that the exact structure of the layers below the active region has little effect on the response. Detectors with various sizes were fabricated, from 10µm to 100µm. They were measured in the UV and in the EUV using different facilities: EUV radiations due to intense optical pulses in gases or in synchrotrons (Soleil and Bessy). It was found that in the 50-150nm range, the measured

photocurrent is strongly dependent on the measurement configuration, and varies little with applied bias. This points towards electron photoemission in the vacuum. Hence, spectral measurements are not very reliable in this range. At shorter wavelengths, the response is measured in a reliable way, as shown in Fig.1. The response increases at short wavelengths as the absorption coefficient decreases and electron photoemission decreases. In addition, multiexcitation processes increase with photon energy.

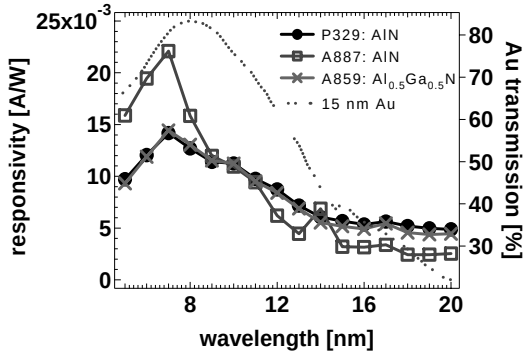

Fig. 1: Spectral response of MSM detectors in the EUV in front side illumination

2.2. Schottky detectors

Schottky detectors are based on a Schottky contact on an undoped (lightly) material and an ohmic contact on an n doped material. For single pixels, front side illumination can be used. A thin Schottky contact is used so as to be transparent to incident photons, and the ohmic contact is taken in a recessed mesa. Electron hole pairs are created just under the Schottky contact which can efficiently collect holes while electrons are collected by the bottom n layer. Fig.2 shows the spectral response of such a diode based on GaN. In the UV, the cut off wavelength is given the Al content, 0% in the present case. In the EUV, the response is quite low from 50 to 150 nm due to the very large absorption coefficient leading to electron photoemission and also surface recombination.

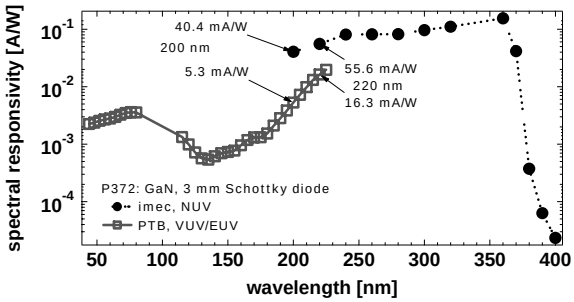

Fig. 2: Spectral response of GaN Schottky detectors in the EUV in front side illumination. V=0V.

At low wavelengths, the absorption coefficient decreases and the response increases as shown in Fig.3. The response is dominated by the Au contact transparency in the EUV. It reaches high values due to the multiexcitation processes: in average, a photon with energy hν gives a number hν/(3Eg) electron hole pairs (where Eg is the material band gap energy). Hence, the ideal response should be around e/(3Eg)=0.1 A/W. At a wavelength of 8 nm, the response reaches 0.06A/W, not far from the ideal value, and limited by the Au transmission coefficient as shown in Fig.3.

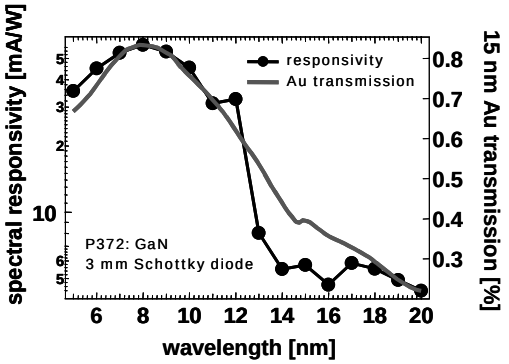

Fig. 3: Spectral response of a GaN Schottky detector in the EUV in front side illumination. V=0V.

3. TWO DIMENSION ARRAYS

3.1. Sample structure

For imaging, 2D arrays must be fabricated. For large arrays with a small pitch, the most practical solution is the front side hybridization of the detector array with a Si read out circuit. Hence, the illumination must be done from the back side. This is an easy solution in the near UV: the AlGaN active layer can be grown on sapphire which is transparent in the 200-360nm range where the AlGaN absorbs. In the EUV, this is more complicated as all materials are absorbing. Hence, the active must be very thin, of the order of the absorption length (less than 1 µm). In addition, the nitride layers must be grown on a substrate which can be removed during the process. This is the reason why we have chosen to grow very thin AlGaN layers on Si(111). The thickness has been set to about 400 nm in order to keep a reasonably good material quality and also for mechanical stability as will be explained later.

The second issue is related to the ohmic contact. In a lateral geometry, a conductive bottom layer is needed for the ohmic contact. In the EUV, this layer will absorb most of the light and electron hole pairs will recombine in the doped material. We propose two solutions to this problem. First, we propose to invert the structure and grow the doped layer on top of the undoped layer. The ohmic contact is taken on the surface while the Schottky contact is taken in a recessed area on the undoped material. The structure can also be viewed as a an asymmetric MSM structure, where one contact is a common contact to all pixels (grid of metal lines deposited on doped material around the pixel). The second solution is to use a vertical structure with a thin back metal contact. This is possible only at wavelengths where the metal is sufficiently transparent. The asymmetry between contacts (nature of the metal) garanties a response at zero bias. In addition, applying a bias (even small) will largely increase the response. Both solutions have been implemented.

3.2. Epitaxy

AlGaN layers were grown on Si(111) with molecular beam epitaxy. The Al content was in the range of 50% as a result of a compromise. Increasing the Al content allows to decrease the cut off wavelength and reach a higher spectral selectivity. However, this is at the expense of the mobility and diffusion lengths, and thus of the collection efficiency. Also, the Al content was varied inside the layer in order to optimise the performance (collection of carrier, quality of the ohmic contact, Schottky barrier height). The layers were grown crack free, with a smooth surface, and a dislocation density in the 10^{10} cm^{-2} range, which is quite high but unavoidable for very thin layers grown on a foreign substrate.

3.3. Process

Two types of arrays have been fabricated. The first one is a 320x256 with a pitch of 30µm so as to be compatible with a commercial read out circuit (Indigo ISC9809). This allows to perform conventional imaging. The second one is a 256x256 with a 10µm pitch. In this case the read out circuit is a switching matrix which allows to read sequentially all column and allow to perform imaging, but not in real time(which is not a problem for the evaluation of the performance). Fig.4 shows the realization of such small pixels (10µm period).

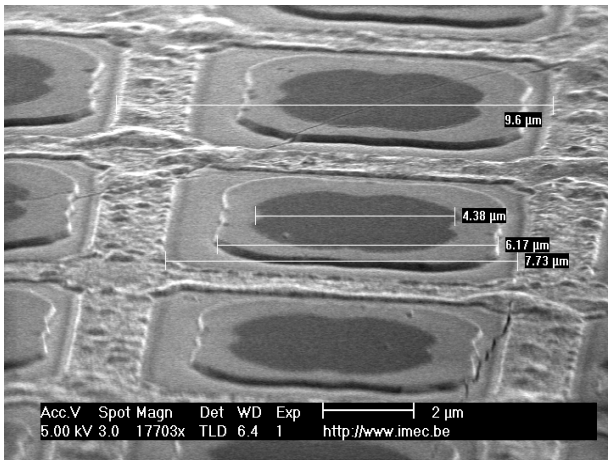

Fig. 4: SEM picture of 10µm size pixels fabricated on AlGaN layers.

In both cases, the process is as follows. After epitaxy, the Schottky diodes are fabricated on the front side of the AlGaN layers. Then the array is hybridized on the Si circuit by In bumps. Finally, the Si substrate is removed by plasma etching. Some silicon was left around the array for mechanical stability. In some cases, we also left some Si lines in the array (reducing the filling factor) in order to increase the stability. This turned out to improve the fabrication yield but was not strictly necessary: membranes as thin as 400 nm and as large as about $1cm^2$ could be fabricated, the stability being due to the periodically spaced In bumps (every 10 or 30 µm)

3.3. Results

First, we observed that the electrical IV curves of the didoes were not degraded by the Si removal. We even observed that the dark current decreased after Si substrate etching. Second we observed (Fig.5) that the spectral response of the array was similar to the response of single pixels measured under back side illumination, showing the the Si circuit was not playing any role in the response.

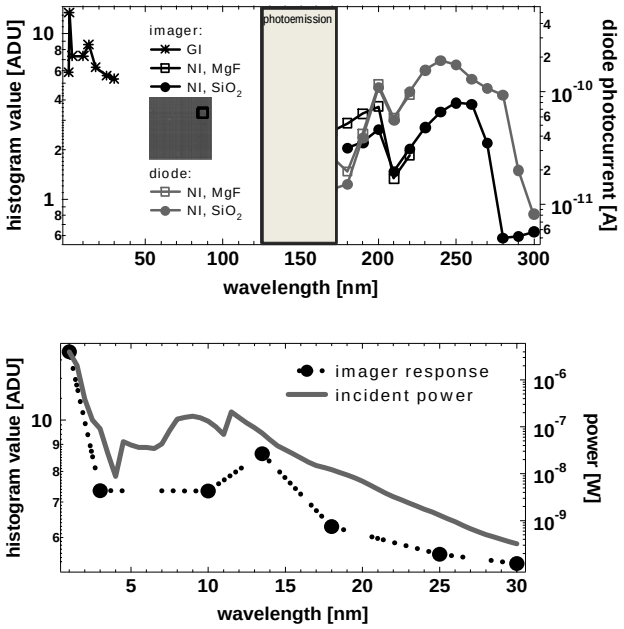

Fig. 5: Response of AlGaN arrays in the EUV. Top figure compares the imager and the single didoe response. Bottom figure is a zoom of the spectrum for very short wavelengths.

The response is quite high at short wavelengths, and weaker in the 50-150nm rage, as already observed in front side illumination, the reasons being the same.

The 320x256 array was integrated in a camera, with all the necessary electronics to perform imaging. The whole system is portable and driven by a PC. The camera is mounted on a flange and can be operated in vaccum to EUV measurements (Fig.6).

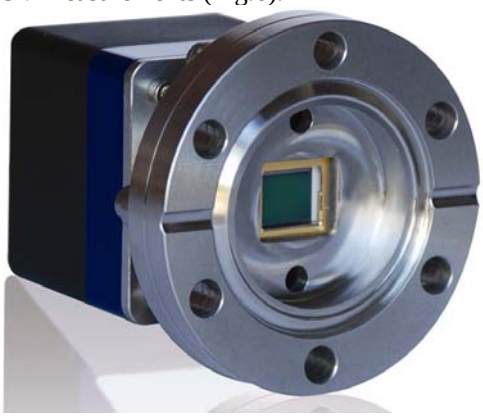

Fig. 6: Prototype camera working in the EUV range.

The spectral response of the camera has been measured at Soleil synchrotron facility and is shown in Fig.7.

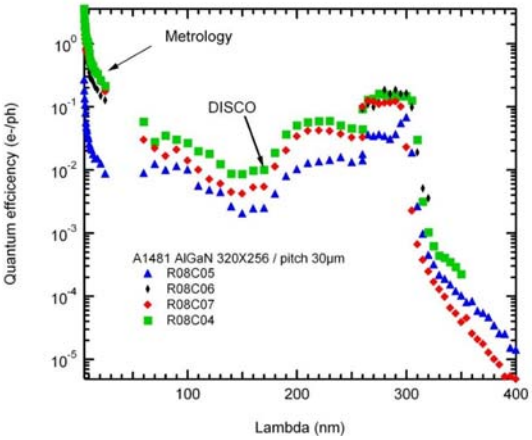

Fig. 7: Spectral response of the camera based on an AlGaN array hybridized to a 320x256 read out circuit.

We again observe the very good rejection ratio for wavelengths larger than 300nm, the large response in the near UV from 300 down to 200 nm, the weaker response region around 150 nm and the large response at very short wavelengths.

This camera was actually used in order to monitor the beam in synchrotron facilities, as shown in Fig.8.

Fig. 8: Image of the split beam of Soleil DISCO line taken at 130 nm by the EUV camera

In terms of performance, the noise turned out to be dominated by the noise due to the read out circuit. More precisely, the noise was due to the switching of the capacitance and was equal to about 150 electrons rms for an integration time up to 100 ms.

4. CONCLUSION

Detectors and arrays of detectors have been fabricated and measured from 1 to 400 nm. AlGaN layers grown on a Si substrate were used in order to produce, at the end of the process, thin membranes that can be illuminated from the back side and can detect EUV light even when the absorption coeffcient is large. In particular, even for the Lyman α line, where the absorption coefficient is highest, we could demonstrate imaging that is highly usefull for beam monitoring in synchrotron facilities. Portable prototypes have been fabricated which could be commercialized. These results clearly establish the state of the art in the domain of EUV detection based on nittrides, both from the scientific and the technological points of view.

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(In,Ga)N PHOTODETECTORS AND APPLICATIONS IN BIOPHOTONICS

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ABSTRACT

(In,Ga)N photodetectors (PD) for VIS and near UV applications are presented. Bulk InGaN regions and InGaN MQW, as well as GaN layers grown on non-polar surfaces have been investigated as active regions. Optimized structures have been fabricated. Their high temperature behavior has been studied and compared with state-of-the-art Si photodetectors. The specific detectivity *D** was taken as comparison parameter. Applications in fluorescence for O_2 sensing by surface functionalization with Ru-based dyes will be introduced.

1. INTRODUCTION

Our R&D activities on (In,Ga,Al)N photodetectors have been driven by applications in high temperature optoelectronics, biophotonics, and polarization-sensitive detection. Combustion control via flame spectral analysis and most fluorescence applications require detection in the near UV-A and VIS ranges. The high performance and low cost of Si photodetectors make it difficult for III-N detectors to have a niche. It will only be feasible if devices have to work in high temperature environments, if they offer extra functionalities, and/or if their integration with needed optical emitters, filters and front-end electronics is clearly advantageous.

2, InGaN MQW PHOTODETECTORS

Bulk InGaN regions and InGaN MQW, as well as GaN layers grown on non-polar surfaces have been investigated as active layers for photodetection. InGaN layers have shown problems like In clustering, high carrier concentration near the surface or nano-scale inhomogeneities, leading to smooth absorption edges and bad rectifying contacts in bulk-based devices. A set of $In_xGa_{1-x}N$ samples was grown by PA-MBE in our institute, covering the whole range of In contents. Besides standard optical and structural characterization, RBS experiments under channelling conditions were conducted. It was confirmed that, in our samples, crystal quality decreases significantly in the $0.3<x<0.8$ range, evidencing the limited miscibility of the binaries [1].

To circumvent above difficulties, metal-insulator-semiconductor (MIS) structures were fabricated on InGaN layers.
PECVD SiN and anodically-grown (In)GaO films were used as insulators. To improve rectifying properties of Schottky contacts on InGaN, compensation of high residual electron concentration by Mg doping was also studied. A detailed study of Mg doping of $In_{0.18}Ga_{0.82}N$ was carried out, obtaining an activation energy of 60 meV for Mg acceptors [2].
Photodetectors based on MQW (Al,In,Ga)N/GaN were considered as an alternative in order to overcome these technological problems. GaN/InGaN MQW active regions for photodetection in the VIS and UV have been used in an attempt to exploit their improved electrical and optical properties, and to benefit from their intrinsic electric fields to obtain internal gain in P-MQW-N devices and improved photovoltaic response in N-MQW-P structures (Fig.1). MBE structures were fabricated at UPM, and thanks to the collaboration with TopGaN-Warsaw, p-InGaN/MQW-n detector structures were also fabricated by MOVPE. Optimization studies were carried out concerning electron blocking layer (EBL), its composition and width, barrier doping and thickness, and number of active QWs. In optimized devices based on $In_{0.2}Ga_{0.8}N$ MQW, detectivities of $D^*= 1.4\times10^{12}$ cm·Hz$^{0.5}$/W were achieved [3].

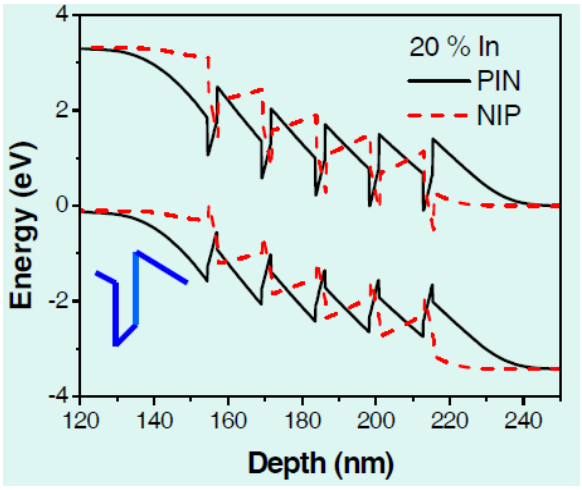

Fig. 1: A comparison of the schematic band diagrams of P-MQW-N and N-MQW-P photodetectors. In N-I-P structures, the higher electric fields in the QW (polarization adds to junction fields) allows a higher PD responsivity.

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(c)presently at: Instituto Tecnológico e Nuclear, Lisbon, Portugal

3. FLUORESCENCE APPLICATIONS

In relation to photodetectors suitable for fluorescence applications, the integration of emitters, optical filters and detectors was addressed, but due to the decomposition of InN at GaN growth temperatures, only hybrid integration by wafer bonding was achieved. On the other hand, surface functionalization of n- and p-type GaN with luminescent molecular probes to achieve chemical sensing features was explored. In collaboration with the Organic Chem. Dpt. of Universidad Complutense de Madrid, Ru-based O_2-sensing fluorophores were selected to prove the feasibility of such concept. A functionalization sequence based on GaN surface oxidation, silanization with 3-aminopropyltriethoxysilane (APTES), and final reaction with the sulfonyl chloride of the luminescent complex, leads to the sought covalent attachment of the O_2 indicator dye via formation of a strong sulfonamide bond. After functionalization of the GaN surface with the Ru complex, the analysis of XPS spectra demonstrated the covalent binding of the luminescent indicator to a GaN surface [4]. Standard GaN/InGaN blue LED chips were functionalized (top p-type surface), and exposed to an O_2 atmosphere. A decrease of the luminescence lifetime with increasing O_2 concentration (Fig. 2) was confirmed.

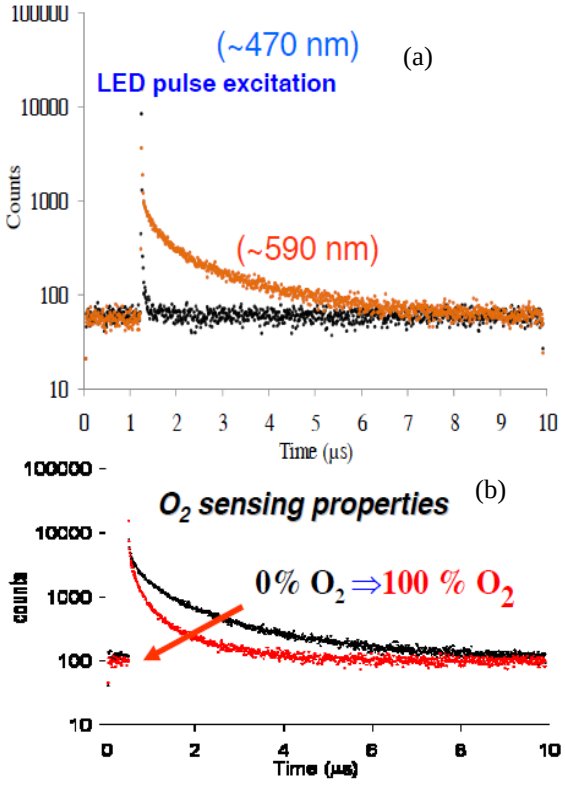

Fig. 2: In (a) the time decay luminescence (590nm) from excited Ru-based dye bound to the chip p-type surface is shown; in (b) the presence of O_2 quenches the luminescence from the Ru-based dye by an electron transfer mechanism to the p-type layer.

4. GaN POLARIZATION SENSITIVE PD

Polarization sensitive photodetectors were fabricated on A-plane GaN grown at UCSB by LP-MOVPE on an R-plane sapphire substrate. XRD showed that the sample was under overall biaxial compressive strain. The high resistivity found in the A-plane GaN material led to fabricate MSM devices. For a single photodetector, a maximum polarization sensitivity contrast of 1.8 and a spectral separation of approximately 2 nm was obtained [5].

5. HIGH-T CHARACTERIZATION

The high temperature behavior of GaN p-i-n, InGaN p-i-n and p-InGaN MQW-n detectors was studied and compared with state-of-the-art Si photodetectors. The specific detectivity D^* was taken as comparison parameter. For visible detection, the advantage of MQW-based devices was demonstrated at working temperatures higher than 50ºC (Fig. 3).

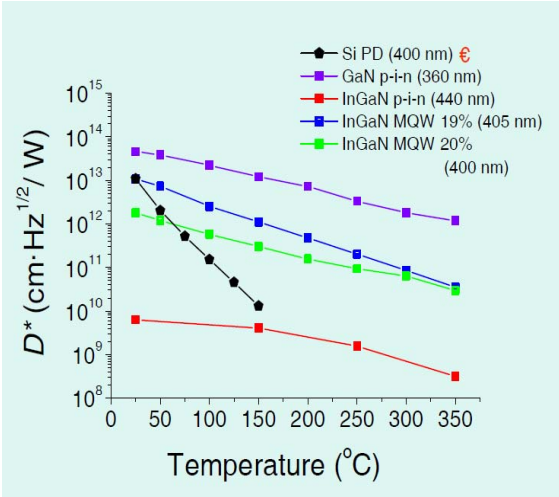

Fig. 3: Detectivity vs. Temperature for a series of InGaN-based PD and comparison with a state-of-the-art Si PD. Homojunction GaN and InGaN MQW PD show the best performance. At 150ºC Si PD has degraded its detectivity by three orders of magnitude.

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INFLUENCE OF P+ LAYER PARAMETERS ON 4H-SiC UV PiN PHOTODETECTOR CHARACTERISTICS

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ABSTRACT

This paper presents a study of 4H-SiC UV photodetectors based on p^+n thin junctions. Two kinds of p^+ layers have been implemented, aiming at studying the influence of the junction elaborated by the ion implantation process (and the subsequent annealing) on the device characteristics. Aluminum and Boron dopants have been introduced by beam line and by plasma ion implantation, respectively. Dark currents are lower with Al-implanted diodes (2 pA/cm^2 @ - 5 V), giving rise to higher values of the UV/dark current ratio.

1. INTRODUCTION

During the past years there has been considerable interest in systems able to record very low light levels in the ultraviolet range in severe conditions of use. The advantage of Silicon Carbide (SiC) with respect to nitride alloys – the major wide band-gap semiconductor used today in industry – relies on three major points : a low residual doping for epitaxial layers (in the 10^{14} cm^{-3} range and concentrations of residual defects/impurities at least one order of magnitude lower), a high thermal conductivity allowing high temperature operations, and a vey good radiation hardness. It is then possible to use SiC for fabrication of devices capable to operate under extreme conditions. Photodetectors based on SiC allow to obtain good wavelength selectivity in the UV range, without any optical filters.

2. EXPERIMENTAL

The role of the p^+ emitter layer properties has been particularly studied in this paper. Among these properties, the doping and the thickness are thoroughly key parameters for controlling the device reliability. Photodetector simulations based on finite element method were performed, optimizing the design of the thin junctions for improvement of the light absorption and the carrier harvest. We also investigated the technological process giving rise to the dopant introduction into the SiC matrix. The comparison between standard ion implantation and pulsed-Plasma Immersion Ion Implantation (PIII) processes is expected to be fruitful, since PIII technology produced impressive results for Si solar cells in the UV range [1]. To our knowledge, PIII doping has never been carried out in SiC material. 4H-SiC n-type epilayers were either implanted with Aluminum by standard ion implantation at 27 keV, or with Boron by PULSION^{TM} system (pulsed-plasma ion immersion) – B_2H_6 at 8 keV, in order to produce p^+-type layer thicknesses of 30 and 10 nm, respectively. The doses were adjusted for obtaining peak concentrations of few 10^{19} cm^{-3} for Al and few 10^{20} cm^{-3} for B. Each sample was then annealed at 1650°C or 1700°C, aiming at analysing the influence of the annealing temperature on the device characteristics.

A prototype of furnace was used during this work (purchased from VEGATEC^{TM}), consisting in a vertical resistive reactor allied with a lift system. This allows to perfectly control the heating-up and the cooling-down rates, up to ~ 20°C/s. After Al implantations, we observed that a high heating-rate improved the sheet resistance whatever the annealing temperature, and preserved the surface roughness for annealing temperatures lower than 1700°C, which is crucial for thin implanted layers. The heating rate has indeed proven to be an important parameter for controlling the reverse current of the related diodes [2].

3. PLASMA IMPLANTATION IN SIC

We propose to study the combination of PIII with a proper annealing, which should results in thin p^+ implanted layers (lower than 30 nm) particularly suitable for UV photon detection. PIII were performed on PULSION^{TM} (Plasma ion implantation tool from the french company I.B.S.) using N_2 gas. Specificity of PULSION^{TM} is that it uses a pulsed DC polarization and a remote ICP plasma source allowing to work at low pressure (< 1x10^{-3} mbar) with the use of low gas flow rate (< 10 sccm). This helps to minimize parasitic etching or deposition usually encountered on Plasma doping tools.

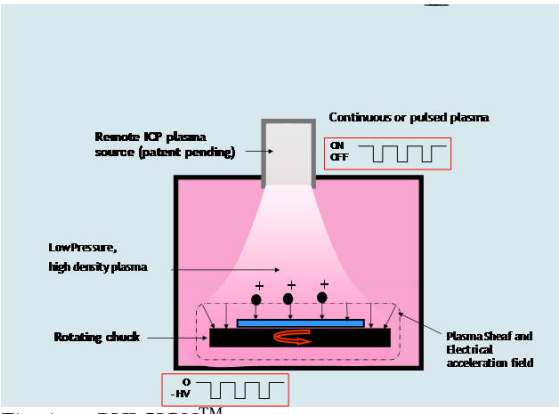

Fig. 1: PULSION™ set-up

A former study proved that, at a given energy, the plasma-process lead to a better surface morphology, a lower bulk defect concentration and a thinner junction than a standard beam implantation process. This is accompanied with some dopant outdiffusion during the annealing, and a higher sheet resistance of the implanted layer [3].

4. SIMULATION

The optical simulation of photodetectors under the UV light have been realised by FDTD method (Finite Difference Time Domain), using the commercial software Sentaurus edited by Synopsys society [4]. Electromagnetic solver based on the FDTD method is used to calculate the electromagnetic field propagation inside UV-photodetector device.

Fig.2 displays the variation of the current density with the reverse bias (with an incident light wavelength at 200 nm), for two distinct p^+-layer thicknesses. In a general way, the current density increases with a thinner junction. When the space charge region is closer to the surface, much more carriers undergoing the electric field are then harvested, leading to a better UV photodetector response.

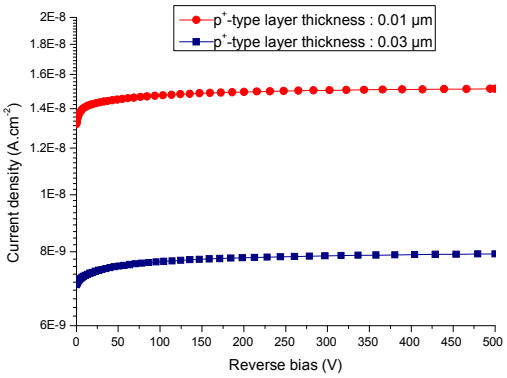

Fig. 2: Current density versus reverse bias at 200 nm with a p^+ doping concentration at $5x10^{19}$ cm^{-3}

5. CURRENT-VOLTAGE

5.1. Hall effect measurements (RT)

The low thickness of Boron-implanted layers impeded any Hall effect measurement. Al-implanted photodiodes lead to the following values of carrier mobility and hole concentration, respectively : 46 $cm^2/(V.s)$ and $2.8x10^{17}$ cm^{-3} for samples annealed at 1700°C, 54 $cm^2/(V.s)$ and $1.9x10^{17}$ cm^{-3} for samples annealed at 1650°C. Rambach *et al.* proved a better activation of Al implanted atoms for a higher annealing temperature, which increases carrier scattering and then diminishes the mobility [5].

5.2. Room-Temperature measurements

The evolution of dark currents with reverse bias is shown in Fig.3. These currents are more important with B-implanted junctions. Some B outdiffusion and/or material etching during the metallization may have partly degraded the junctions.

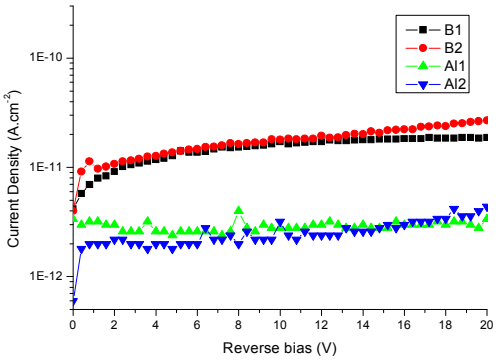

Fig. 3: Dark currents of Al- and B- implanted photodiodes

Characteristics of the diodes have been measured under light, with an incident wavelength of 365 nm. Fig.4 displays the evolution of the UV/Dark current ratio with reverse bias. Again, Al-implanted photodiodes revealed better achievements, proving a ratio six times higher than for B-implanted diodes.

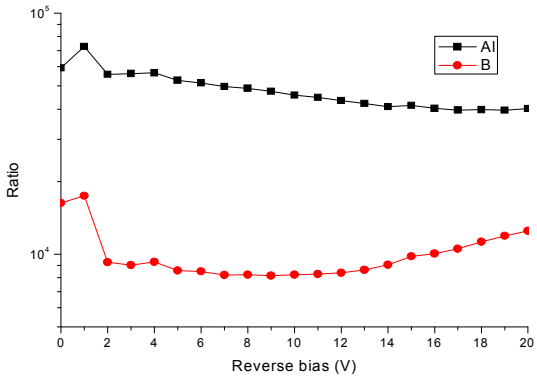

Fig. 4: UV/Dark current ratio for Al- and B- implanted photodiodes

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CHALLENGES OF HIGH-SPEED EUV MASK BLANK INSPECTION

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ABSTRACT

We present the current status of our EUV mask blank inspection demonstrator developed according to requirements of high-volume EUV lithography. Limitations of sensitivity and scan speed, that are caused by source flux, sample movement speed and performance of objective- and detector, are discussed. Furthermore we present alternative detection concepts and discuss their potential to overcome the limits of state of the art backthinned and backilluminated charge coupled devices (CCDs).

1. INTRODUCTION

One of the key prerequisites for the introduction of extreme ultraviolet (EUV, 13.5 nm) lithography is an extremely low amount of critically sized defects on mask blanks. According to the industrial requirements mask blank inspection tools have to be able to detect sub-40 nm defects on a 150x150 mm mask blank in 45 min. Since the detection of buried defects in mask blanks is only possible with at-wavelength (actinic) detection, the inspection system has to overcome a number of challenges, such as slow readout speed of detectors (typically charge coupled devices), limited EUV radiation intensity and the requirement of combining a high resolution with a large field of view.

2. EXPERIMENTAL SETUP

In this work results of the development of an actinic mask blank inspection demonstrator in a dark field mode (Figure 1 and Figure 2) will be presented [1].
The demonstrator consists of an EUV gas discharge source, an ellipsoid ring collector, a deflection mirror, a mask blank holder with 5 degrees of freedom to adjust the sample, a Schwarzschild objective and a backthinned backilluminated CCD camera. For operation in dark field mode, the deflection mirror works as a beam stop for the reflected radiation cone from the mask blank. That way, only scattered light from defects can be detected, due to of its larger scattering angle, compared to the illumination cone.

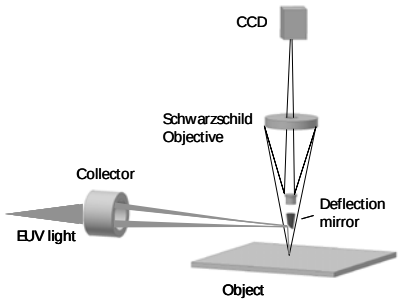

Fig. 1: Scheme of the mask blank inspection demonstrator

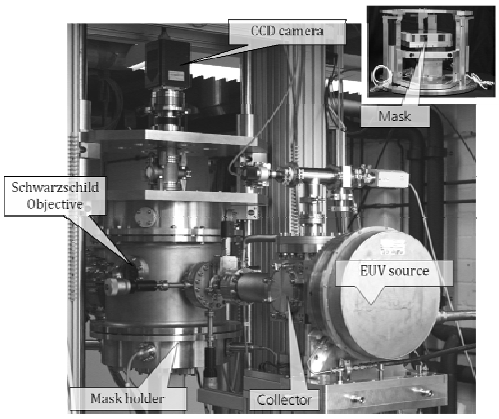

Fig. 2: Photo of the mask blank inspection demonstrator

3. EXPERIMENTAL RESULTS

With the demonstrator several programmed test structures and natural defects on multilayer mirrors have been investigated and cross characterized with an atomic force microscope (Figure 3).

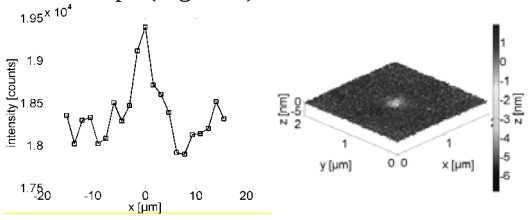

Fig. 3: Natural defect: image profile from EUV demonstrator (left) and atomic force microscope image (right)

The results of the investigations have been used to estimate and validate the parameters that are used in the limitation calculations. The analysis of the experimental results will be presented.

4. DISCUSSION

The performance of an inspection tool is limited by the available source flux, the sample movement speed, the parameters of the Schwarzschild objective and the detector performance. Crucial performance parameters of the tool are the total inspection time and the defect detection sensitivity.
Based on the requirement to detect a sub-40 nm defect, the minimal required magnification of the objective can be calculated. Because the mask blank is not atomically plane plane, the light scattered from the blank´s surface (flare) has to be taken into account. The main parameters influencing the calculation therewith are the scattering and collection efficiencies of defect and flare, the dynamic range of detector, the ratio between pixel- and defect area and the signal to noise ratio.
Based on the requirement to scan a complete mask blank within 45 min, the maximal feasible magnification can be calculated. Here the main parameters are the read out speed of the detector, the light flux of the source and the sample movement speed.
Finally the optimal magnification of the setup that can fulfill both the requirements in sensitivity to sub-40 nm defects and in sub-45 min scan speed, will be presented.

5. ALTERNATIVE DETECTION CONCEPTS

To date the most limiting component in a mask blank inspection tool concerning scan speed and defect detection sensitivity is the detector.
To fulfill the industrial requirements, a different detector is mandatory. Current detectors and detector concepts will be presented and their potentials for mask blank inspection discussed.

5.1. CCD detectors

In the field of CCD detectors there are several different designs, e.g. full frame CCD or frame transfer CCD, which will be discussed. Furthermore time delay integration CCDs will be presented regarding their potentials and limitations [2].

5.2. Wide bandgap detectors

Instead of silicon - the state of the art material of CCD and CMOS detectors – wide bandgap materials can be used. A wider bandgap allows to avoid the detection of visible light, removing the need of spectral filters in the beampath. This simplifies the experimental setup and enhances the available light flux by a factor of approx. two. The main disadvantage is at this time the significantly lower quantum efficiency [3].

5.3. Scintillator composites

Instead of using an EUV sensitive detector, a scintillating material can be placed in front or onto a detector, which is sensitive to visible light. The main advantage is a higher read out speed, by using a complementary metal oxide semiconductor (CMOS) detector, the main disadvantage is a significantly lower quantum efficiency.

5.4. CMOS detectors

5.4.1. Backthinned backilluminated CMOS

State of the art backthinned backilluminated CMOS detector offer comparable quantum efficiencies but not significant higher read out speeds in comparison to state of the art CCD detectors [4].

5.4.2. Open electrode CMOS

A novel CMOS fabrication extension concept called deep optical stack etching offers the potential to provide higher read out speeds, smaller pixel sizes and comparable quantum efficiencies, compared to state of the art CCD detectors [5].

6. CONCLUSION

The presented concept for mask blank defect inspection is principally suited for the industrial requirement of scanning a complete mask blank within 45 min. Current performance limitation are the scan speed and defect detection sensitivity, which are limited by the read out speed and the pixel size of the detector.
The most promising concept to overcome these limitations is an open electrode CMOS concept, which offers higher read out speeds, smaller pixel sizes and comparable quantum efficiencies, compared to state of the art CCD detectors.

ACKNOWLEDGEMENTS

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THE ROLE OF OPERATING CONDITIONS IN THE CHIP-LEVEL DEGRADATION OF WHITE LEDS

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ABSTRACT

The aim of this work is to present the results of an extensive reliability analysis carried out on two different types of commercial white LEDs. In order to analyze the effects of operating current and storage temperature on the electro-optical properties of these devices, iso-thermal, iso-current and pure thermal stress tests were performed for several thousands hours; we used storage and junction temperatures in the range 60-200°C, and current levels in the range 0.5 A - 1.5 A.

The two types of LEDs showed marked differences in the degradation kinetics especially for the electro-optical modifications of the chip.

1. INTRODUCTION

GaN-based light emitting diodes represent the most promising technology in the future of lighting, especially for the white light generation by means of a blue InGaN/GaN chip, coated with YAG:Ce phosphors. Chip-related degradation can significantly limit the reliability of white LEDs, because of the high temperatures and current densities achieved by the junction during the operation. For this reason it was chosen to deeply investigate the effects of high operating currents and high junction temperatures on commercially available power LEDs; selected devices represents the state-of-the-art of the 1W White-LED technology, produced by two of the leading manufacturer.

2. EXPERIMENTAL DETAILS

The devices analyzed during this work are divided in two groups (called group A and group B), and were fabricated by two different manufacturers. All the samples were mounted on a heat-sink and connected by means of 4-wire Kelvin configuration. Several reliability tests were carried out as follows:

- iso-current stresse tests; the samples were placed in various climatic chambers with different temperatures and submitted to an operating current of 1A;
- iso-thermal stresse tests; the samples were stressed at different current levels in the range of 500mA-1.5A; for each set of devices the ambient temperature was adjusted in order to have the same average junction temperature (140°C for the group A and 160°C for the group B); the junction temperature was evaluated by

means of the forward-voltage method described in [1];

- several sets of devices were submitted to purely thermal stresses in the range 85°C-200°C.

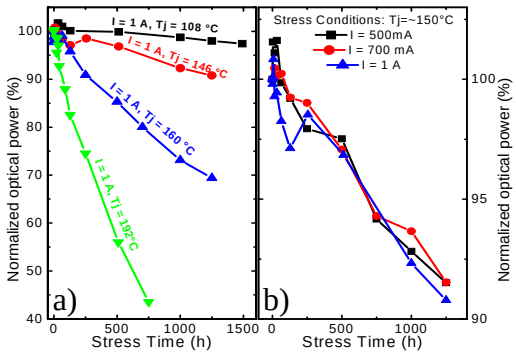

Fig.1: Optical Power degradation measured (at 700 mA) on devices of group A stressed a) at different junction temperature with the same current level, b) at different current levels with the same junction temperature. Each data point is the average of four identical samples.

For each stress condition and each manufacturer group four identical samples were tested.

The electro-optical characteristics of the devices during the stresses were monitored by means of current versus voltage (I-V), optical power versus current (L-I) and electroluminescence (EL) measurements.

3. RESULTS

The two sets of devices showed marked differences in the degradation kinetics and so the results analysis will be treated separately in the following.

3.1. Samples of Group A

Fig.1 reports the comparison between the results of iso-current and iso-thermal stresses carried out on the samples of group A. From this comparison it is clear that the main degradation mechanisms that affect the samples of group A is strongly related to the temperature reached by the junction during operation (see Fig.1a) and not to the current values used for the stresses (see Fig.1b). This relationship is confirmed by the $TTF_{90\%}$ (time necessary for a 10% decrease in optical power) which has an Arrhenius dependence on temperature (Fig.2, blue dots). The Arrhenius plot can be divided in two precise region, with two different activation energies. The first degradation process (Tj<160°C,Ea=0.27eV) takes place due the generation of lattice defects at moderate junction temperature, as previously reported (see [2]-[4]).

The second thermally-activated degradation process (Tj>160°C,Ea=1.1eV) is strictly correlated to the increase in the operating voltage: note the specularity of

the behaviors of $TTF_{90\%}$ and of the operating voltage in Fig.2.

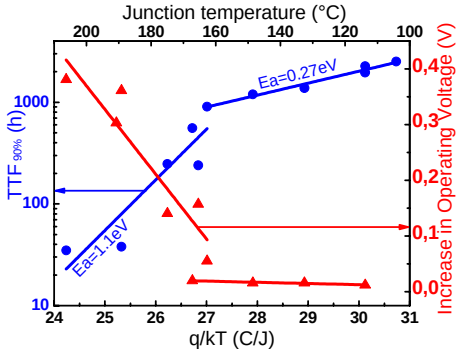

Fig.2: Arrhenius plot of the $TTF_{90\%}$ (blue dots) compared to the increase in operating voltage (red triangles) for the group A iso-current stresses.

This type of mechanism, as described in literature ([5]-[7]), can be associated to the interaction between the acceptor dopant (Mg) and the hydrogen present in the semiconductor or in the passivation layer, activated by high temperature levels, which increases the series resistance (and operating voltage) of the samples, with a subsequent efficiency loss of the LED.

Most of the optical power degradation showed by the devices of group A can be ascribed to chip-level modifications, because the packaging materials (phosphor coating, silicone lens and reflector cup) did not reveal any substantial changes in their optical properties.

3.2 Samples of Group B

Devices of group B showed degradation mechanisms related both to the junction temperature and to the current level used during the tests. The main effect of temperature appears to be the a significant darkening of the plastic reflector cup with a subsequent decrease in the light extraction efficiency (Fig.3a; red line). Purely thermal stress tests did not induce any change on the electrical characteristics of the devices. Fig.3a summarizes all the iso-thermal stresses (160°C), where it is evident the superimposition of the current-related degradation process over the thermally-activated one. Degradation rate was found to have a nearly linear dependence on the stress current level, as shown by Fig.3b.

The analysis of the current-voltage characteristics during the biased iso-thermal stresses reveals an increase in the defect-related current components for low voltage values (Fig.4), which means that the carrier flow induces the generation of non-radiative defects in the semiconductor lattice, with subsequent decrease in the internal quantum efficiency of the device.

The defects formation, and the subsequent generation of parasitic shunt paths is also responsible of a decrease in operating voltage of the devices and of a slight red-shift of emission wavelength of the blue semiconductor chip (not shown here for brevity). The kinetics of both of these processes have the same time constants of the optical power decay, confirming the fact that the electrical modifications of the active region of the device are directly involved in the current-related degradation mechanisms of the examined samples.

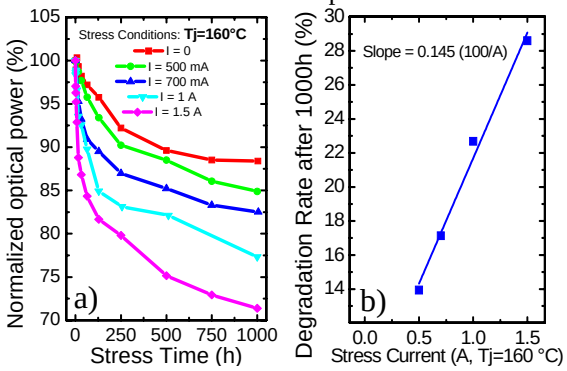

Fig.3: a) Optical Power degradation measured (at 700 mA) on devices of group B. b) Degradation after 1000h for devices stressed at different current levels, same junction temperature (160 °C). Each data point is the average of four identical samples.

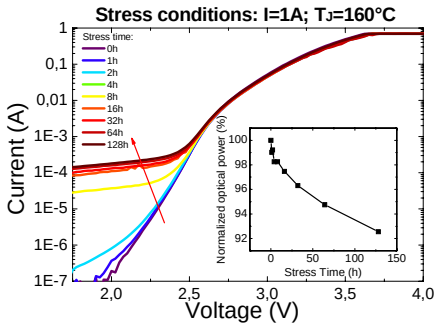

Fig.4: Current-voltage characteristics measured on one of the LEDs of group B stressed at 1A, Tj=160°C. Inset: Optical Power degradation of the same device.

4. CONCLUSIONS

The results presented in this work highlight the role of operating conditions in limiting the reliability of commercial white LEDs; both the current levels and the high temperatures are involved in various types of electro-optical degradation mechanisms: i) the samples of group A have presented two different thermally activated behaviors, both related only to modifications of the blue semiconductor chip (i.e. defects formation and the interaction between Mg and hydrogen); ii) the samples of group B show the superposition of two different optical power decay mechanisms, one thermally activated (the darkening of the reflector cup) and one strictly related to the current level which leads to the generation of non-radiative defects in the active layer of the chip.

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MOCVD GROWN ZnO ON C-PLANE SAPPHIRE SUBSTRATES FOR LIGHT AND GAS SENSING APPLICATIONS

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ABSTRACT

The successful growth of nanostructured ZnO by MOCVD on c-plane sapphire for light and gas sensing applications is described. XRD indicates c-axis orientated ZnO with a strong PL peak at 376 nm. Metal-Semiconductor-Metal (MSM) structures using different metals as anodes have been characterized. Samples grown at 500 °C showed the highest diode response for 405 nm wavelength using Pd or Au as contact. The structures showed gas sensing characteristics with fast response time and a detection limit down to 1 ppm of H_2 at different working temperatures ranging from 250 °C to 360 °C.

1. INTRODUCTION

Photodetectors operating in the short wavelength region (10 to 400 nm) are important devices that can be used in a variety of applications. The study reported here points out the advantages of Zinc oxide (ZnO) as promising candidate for UV detection. It also confirms its superiority with respect to Si-based optical photodetectors, which show comparably weak UV sensitivity and strong response to visible and infrared radiation due to the 1.2 eV bandgap of Si [1-3]. ZnO as a direct bandgap (Eg= 3.36 eV) semiconductor with a large exciton binding energy (60 meV), exhibits near UV emission, transparent conductivity and piezoelectricity. ZnO is bio-safe and biocompatible, and may be also used for biomedical applications [4]. Furthermore gas sensors based on ZnO have attracted much attention due to their chemical sensitivity to volatile and other radical gases [5-8]. The great interest in the development of hydrogen sensors for applications such as leak detection and fuel storage systems points out the need for reliable gas detection devices [9, 10]. Sensors consisting of nanostructures with large surface area to volume ratio have better response characteristics and higher sensitivity making them attractive for sensing applications.

2. EXPERIMENT

ZnO nanostructures have been synthesized using Metal Organic Chemical Vapor Deposition (MOCVD). The material has been characterized using SEM, PL and XRD. The structural quality was monitored by in-situ interferometry during growth [11]. MSM sensors with different contact electrodes were fabricated on ZnO layers grown at 500 °C and 600 °C. A circular structure of e-beam evaporated Au, Ag, Pd, Pt metals was used as anode and Ti/Al/Ti/Au was used for low resistance ohmic contact cathodes. The diameter of the anode and cathode was 1100 µm and 2600 µm respectively, while the gap between the two contacts was 100 µm. The devices were measured under illumination of different laser sources and their reverse current characteristics were compared with those obtained under dark conditions. The wavelengths used were 650 nm, 532 nm and 405 nm. The measured corresponding laser power was 4, 13 and 15 mW/cm² respectively. In addition to light sensing characterization, we evaluated the hydrogen gas sensing characteristics of the structure in synthetic air and nitrogen by applying different concentrations of diluted hydrogen to the sample. The sample was mounted on a commercially available micro-heater (Heraeus MSP 632). The dissociation efficiency of molecular hydrogen to the atomic form could be increased by heating the sample from the backside.

3. RESULTS

1 µm thick ZnO has been deposited using an Aixtron 200/4 MOCVD system. The growth rate has been calculated to be ~1.2 µm/h based on in situ interferometer results and SEM thickness measurements.
The layers contained homogenous ordered nanostructures as confirmed by SEM shown in Fig 1. By way of comparison, growth at 600 °C resulted in porous ZnO layers and milky features as confirmed by the fast decay of the interferometry signal during growth. Higher growth temperature results in less dense structures and rougher surface morphology. XRD confirmed the high c-axis orientation of the samples. A near band emission around (376 nm) and comparable weak green band emission for both samples could be confirmed by means of photoluminescence.

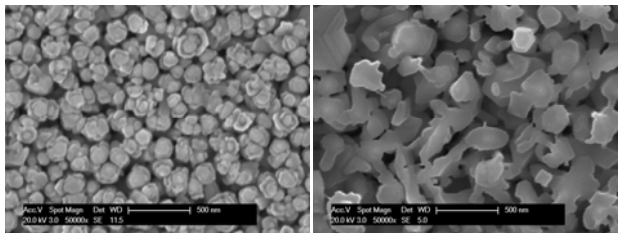

Fig. 1: SEM pictures of ZnO on Sapphire grown at 500 °C (left) and 600 °C (right).

3.1. Photo Sensors

The best diode response was found to be under blue laser illumination and the corresponding reverse current was two orders of magnitude higher compared with the current measured under dark conditions. The highest measured current was observed for Pd and Au contacts and was by a factor of ~135 higher than the dark current. The samples grown at lower growth temperatures had a response to blue light illumination which was two times higher compared with high temperature grown samples. The response to red or green laser light was up to one order of magnitude lower compared with that measured using the shorter wavelengths of blue light. The approximate normalized sensitivity over the total area of the device is shown in Fig. 2. The photoresponse of the sample is in the range of seconds and can be mainly attributed to the creation of holes by illumination and detrapping of negative defect induced charged oxygen ions near and on the surface and transit to electrodes [12].

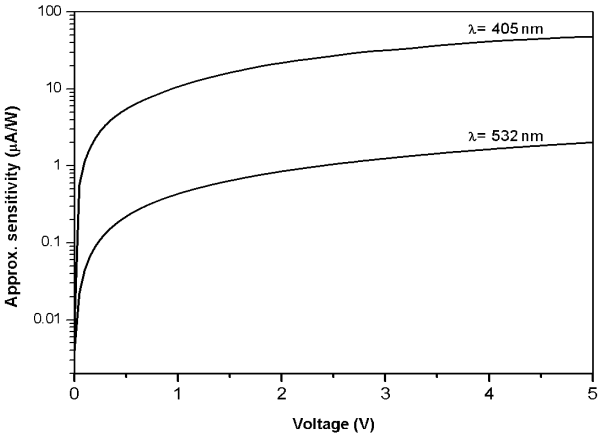

Fig. 2: Sensitivity of the ZnO photodetector for applied green (532 nm) and blue (405 nm) laser light using Pd as anode metallization.

3.2. Gas Sensing Characteristics

The samples showed excellent gas sensing characteristics at temperatures higher than 250 °C. Due to chemisorbed oxygen on the ZnO surface, a depletion region is formed on the film surface and at the grain boundaries resulting in case of n-doped ZnO in conductivity decrease [13]. By applying hydrogen gas to the sample the current increases due to oxygen originating from the sample and absorbed on the nanostructured ZnO surface. As shown in Fig. 3 the detection limit was 1 pppm with a corresponding change in resistance of 10 %. A noticeable low response time in the order of tens of seconds and a high reproducibility could be confirmed by repeated measurements. Due to the high resistivity of the material the power consumption of the device is relatively small (< 50 μW).

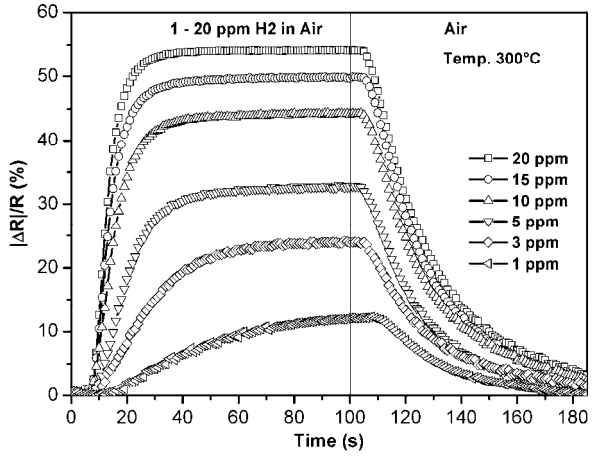

Fig. 3: Gas sensing properties for MSM semiconductor gas sensor using Pd as anode metallization with an applied bias voltage of 1 V.

4. CONCLUSIONS

In summary we present here the use of ZnO nanostructured samples for optical and gas sensing applications. The samples showed the highest photo response for shorter wavelength (405 nm) while being relatively insensitive for longer wavelengths. These effects can in general be dedicated to defect induced traps. Measured gas sensing characteristics demonstrated an excellent low detection limit for hydrogen sensing, fast response times and low power consumption.

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MULTI-WAVEGUIDE NEEDLE PROBES AND INTEGRATED LASER DIODES FOR OPTO-GENETIC NEURAL APPLICATIONS

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ABSTRACT

Optically sensitive proteins (opsins) have recently been developed that can be incorporated in neuron cell walls by harmless viruses so the neurons can be activated and silenced by specific colors of light (e.g. blue, and yellow or orange, respectively). This discovery has given rise to a need for needle probes to deliver optical signals to target tissue regions, and for laser diodes (LDs) at new wavelengths to power them. To this end silicon-based light delivery probes with parallel silicon oxy-nitride waveguides running down their narrow shank have been produced to deliver light to multiple points within living tissue. Orange/amber platelet laser diodes are being developed for integration with these probes.

1. BACKGROUND AND INTRODUCTION

Optical control of neural activity is a new tool that is finding wide application in neuroscience, with hundreds of labs using this technology to activate and silence neural circuits and cell types *in vitro* and *in vivo* in a variety of species. The recent discovery of molecules that can act as genetically-targetable optical sensitizers, such as channelrhodopsin-2 (ChR) and halorhodopsin (Halo/NpHR), are enabling many new basic science question to be answered by probing the causal contribution of specific cell classes to neural computations [1,2]. Improved opsins, i.e. molecules for these purposes, are continuing to be discovered [3].

When these molecules are expressed in a specific cell class, illumination of brain circuits will selectively activate or inhibit that cell class, for milliseconds at at time, leaving other cells and fibers of passage unaltered. Furthermore, such molecules function safely and efficaciously in the non-human primate brain, suggesting potentially revolutionary clinical uses of cell type specific optical neural stimulation that maximize efficacy while minimizing side effects [4].

Hardware for cell-type specific optical neural control has lagged behind the molecular advances however. To meet this need we have designed, fabricated, and characterized silicon-based light delivery probes (see Fig. 1) engineered to deliver light to multiple points within living tissue, as will be described in Sec. 2. We are also extending micro-scale hybrid integration techniques we have developed for heterogeneous integration of laser diodes on silicon substrates [5,6] to create compact multi-color laser diode array sources for integration with these probes. However, the major challenge in this work is not integration, but rather producing laser diodes at the wavelengths required. Research begun to address this problem is described in Sec. 3.

2. MULTI-WAVEGUIDE NEEDLE PROBES

The main challenges in producing a probe suitable for delivering different light signals to distinct tissue regions along its length include integrating multiple optical waveguides on a narrow, e.g. 200 μm wide, needle, while

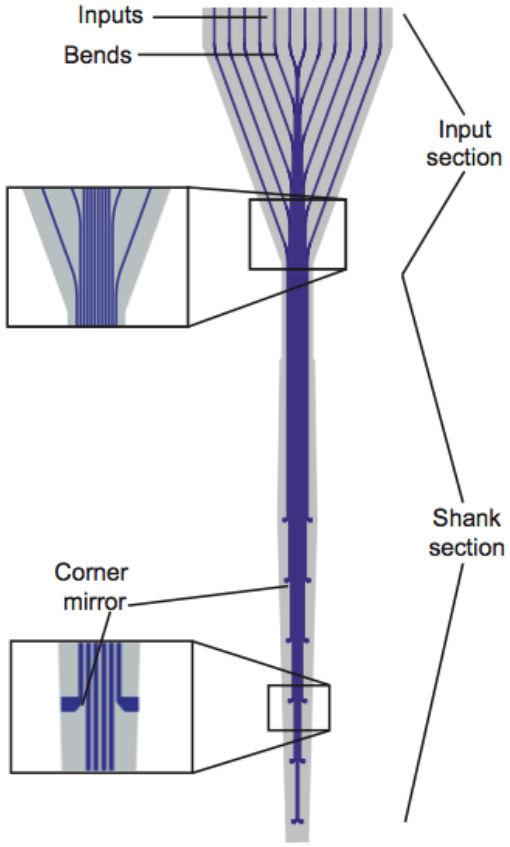

Fig. 1: A drawing illustrating the layout and features of a representative multi-waveguide optical probe. Of particular note is the novel corner mirror design, which provides lateral emission from the sides of the narrow probe, without adding appreciably width. The overall length is 1.5 cm.

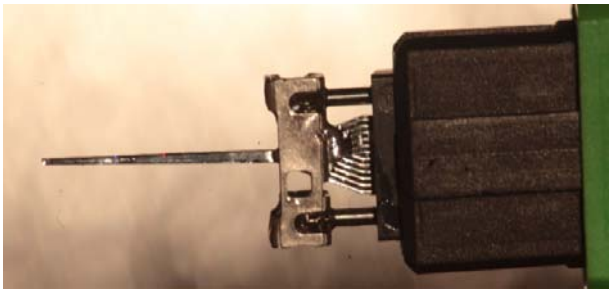

Fig. 2: A photograph of a completed probe mounted on a standard ribbon-fiber ferrule mated to a companion connector on the end of a ribbon-fiber. The probe extending to the left beyond the ferrule is approximately 1 cm long.

also providing efficient macro-scale inputs to each guide, and terminating each guide at an exit port projecting light laterally from the edge of the probe into the surrounding tissue. To meet these challenges, rectangular cross-section silicon oxy-nitride waveguides are patterned on a silicon oxide lower cladding layer on a silicon wafer. A SiO_2 side and upper cladding are then deposited over the patterned guides, and a coating of aluminum is deposited over the entire surface. Light in the waveguide core is shielded from this Al by the cladding in most of the structure, but near the exit where a facet has been patterned at a 45˚ angle to axis of the waveguide, the Al on this facet reflects the light in the guide laterally out the side of the probe, and into the surrounding tissue [6]. This structure, which is a key contribution of this work, is shown as an insert in Fig. 1. A complete waveguide probe with 12 parallel SiO_xN_y waveguides is shown in Figs. 1 and 2. The guides along the probe shank are 20 µm wide and are 10 µm apart. In the probe pictured, the exit ports are 1 mm apart on both sides of the probe. The waveguides bend and separate in the upper region of the probe to create 10 by 20 µm input ports spaced with a 125 µm period to match a standard ribbon fiber cable.

The probes are presently mounted on a ribbon-fiber coupling ferrule, as seen in Fig. 2, and this ferrule mates to the output ferrule of a 12-fiber ribbon cable (visible to the right in Fig. 2). Each fiber in the ribbon is connected to a discrete laser source that supplies one of the twelve optical signals. Ultimately, however, we need a more compact assembly with laser diodes (LDs) integrated with drive and control electronics on a Si chip that can be mated directly to the probe. Integrating LDs on Si is not difficult, as we have demonstrated earlier in WOCSDICE 2009 and in the literature [5], and those same techniques will be used here. The bigger challenge is making LDs at the required wavelengths, which is difficult. Red laser diodes are readily available, and blue laser diodes are becoming more so, but in between little is available.

3. VISIBLE PLATELET LASER DIODES

The excitation spectrum of an important opsin, halorhodopsin (Halo/NpHR), or simply "halo", is shown in Fig. 3. As is typical of many current opsins, the highest sensitivity is in the mid- and upper-visible spectral range. One objective of current work on opsins is to find molecules with excitation spectra shifted more

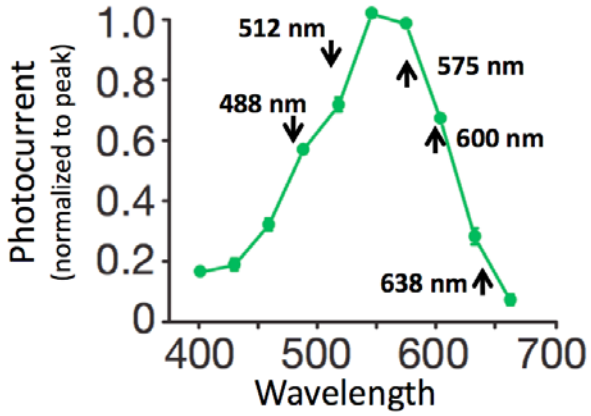

Fig. 3: The excitation spectrum of halorhodopsin, with the target new LD wavelengths (575 and 600 nm) indicated. Also indicated are existing LDs at 488, 512, and 638 nm.

to lower energies, and halo is an important starting point because it already has unusual orange sensitivity.

Practical yellow and orange LDs do not currently exist. In fact, little work has been done on yellow and orange laser diodes since the mid-1990's [7]. Since then commercial InGaAlP red MQW LDs have been improved significantly, and orange and yellow LDs should benefit from these advances. With this belief, InGaAlP MQW laser diode heterostructure wafers designed for 575nm and 600nm emission have been ordered from a foundry [8]. These structures are based on commercially supplied red laser structures adjust for these wavelengths, and with an underlying etch-stop layer for substrate removal and platelet laser processing.

4. FUTURE DIRECTIONS AND APPLICATIONS

Integrated LDs are viewed as an important long-term goal because they will enable minimally tethered animal studies, but they will take time to develop. Shorter-term, more readily achievable goals include integrating sense electrodes onto the waveguide probes, and fabricating linear arrays of optical probes, and then 2-dimensional arrays, for 3-d volume activation. Customized versions of single probe like the one in Fig. 2 are also be produced for use by collaborators for animal studies.

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ALL-IN-ONE DESIGN OF INTEGRATED 1X2 TE/TM POLARIZATION SPLITTER/COMBINER/CONVERTER ON InGaAlAs-InP

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ABSTRACT

An innovative architecture for integrated polarization controller on InGaAlAs/InP based on a novel coupled hybrid supermodes waveguide, having a 50dB TE-to-TM extinction ratio and 99% conversion ratio, has been demonstrated by 3-D simulation.

1. INTRODUCTION

Integrated optical polarization controllers (PCs) has become more important in developing photonic integrated circuits (PIC's) for high capacity optical transmission system, e.g., in the 100Gb/s system based on dual-polarization quadrature phase shifting keying modulation and polarization diversity [1]. Basically, key elements of PCs for using in all these applications can be divided into two classes - polarization converter and polarization splitter/converter. Considering only one of either can be achieved in usual, therefore, how to develop PCs having all-in-one abilities is always an issue. Despite many approaches for realizing PCs has been proposed [2]; however, efficient designs for easily integrating PCs into active devices (e.g., laser, SOA, photodetector, etc.) are still quite limited. On the other hand, people always face more challenges on design and fabrication from polarization converter rather than polarization splitter/converter. One solution for polarization converter integrated on InGaAsP/InP presented by Augustin et al. [3] is made by a slanted ridge waveguide with a precisely controlled slope and angle. Then, they cascade two polarization converters into both arms of Mach-Zehnder interferometer to realize splitter/combiner by interference effect. However, this device requires two subsequent different etching steps (dry and wet etching) with helping by two kinds of lithographical technologies (electron beam and optical stepper), making the production process rather difficult. Therefore, we aim to present a whole new architecture as Fig. 1 for simultaneously reaching those key functions of controlling polarization – splitter, combiner and converter on InGaAlAs/InP SOA epi-structures, but specific fabrication skills are unnecessary.

2. PRINCIPLE AND DESIGN

The key idea for this proposed layout as Fig. 1 is focused on how to glorify the advantage of hybrid supermodes (HSM) for controlling states of optical polarization.

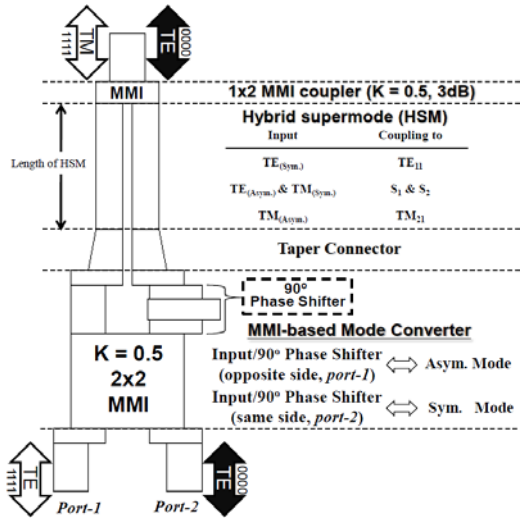

Fig. 1. Layout of the 1x2 TE/TM polarization controller.

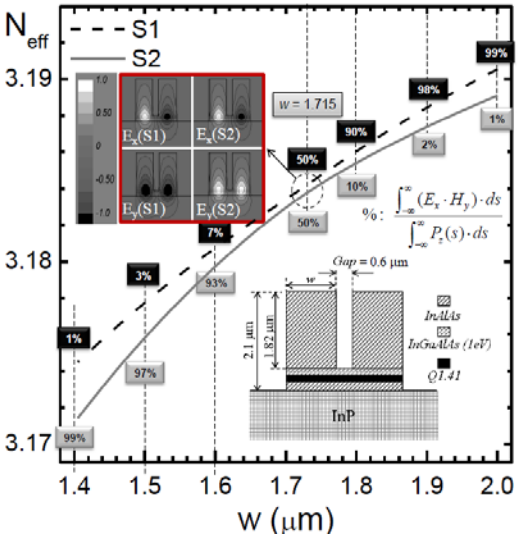

Fig. 2. Mode effective index vs. width of HSM waveguide. (Inset, top/left: E-field profile when w = 1.71μm, bottom/right: Cross-section of coupled HSM waveguide)

In general, a HSM waveguide is designed to maintain three modes at least (one fundamental TE-mode & two hybrid supermodes). HSM means the field of optical mode (E-field or H-field) will be not only hold on one direction (horizontal or vertical). In other words, they have a very strong hybrid character (*i.e.* E_x is as strong as E_y and vice versa); meanwhile, they can be excited simultaneously due to the degeneracy. However, in order to attain a fundamental mode at the output, polarization

converter made by a strip HSM waveguide will sacrifice half of the launching intensity essentially in application [4]. In this study, the epitaxial slab waveguide on InP substrate is assumed to have a 1.82-μm thick (mostly InAlAs) upper cladding, a 0.14-μm thick core layer containing 3 quantum wells with the absorption edge at 1.41-μm, and a 0.14-μm thick lower cladding (also mostly InAlAs). Here, we use a coupled waveguide structure to construct a fine-tune HSM waveguide. As Fig. 2 inset show, we can find out an exact structure for HSM by changing etching depth, width (*w*) and separation (*Gap*). Fig. 2 indicates the simulated evolution of mode effective index vs. "*w*" in wavelength = 1.55-μm (the base wavelength in this study) when "*Gap*" and depth are separately fixed to 0.6-μm and 1.82-μm/2.1-μm (outside/middle). It helps us to indentify HSM degeneracy region as pointed by circle. Further, we check the fraction of the Poynting vector with field in horizontal as marked by "%" for understanding the width tolerance from optimum condition of HSM (50%/50%). Top-left inset of Fig. 2 shows those E-field profiles of both hybrid modes (S1&S2) when *w* = 1.71-μm, it hints this coupled HSM waveguide can only be excited by symmetric TM mode (TM_{Sym}) and asymmetric TE mode (TE_{Asym}). Hence, in case of launching one of either of TM_{Sym} and TE_{Asym} modes, both of S1 and S2 will be excited together, we can therefore rotate E-field by increasing the length of HSM waveguide; meanwhile, achieving a 90^0 rotation (TE/TM converter) once the length of HSM is equal to $L_\pi = \pi/(\beta_{S1} - \beta_{S2})$ ($\beta_{S1,S2}$ are the propagation constants of S1 and S2). In case of the 90^0 rotation, optical mode will be changed into TM_{Sym} if launching TE_{Asym} and vice versa. In Fig. 1, except HSM waveguide, a route-sensitive mode converter, formed by cascading a 2x2 3dB multimode interference (MMI) and a specific 90 degree phase shifter, is then introduced to this structure; simultaneously, it is connected to HSM waveguide by a pair of taper connecter. Finally, a 1x2 3dB MMI coupler is introduced into its end. The use of MMI couplers allows large fabrication tolerance, low excess loss, large bandwidth and low polarization sensitivity.

3. RESULTS AND DISCUSSION

By this design, to control polarization state of TE/TM wave with functions as highlighted in Fig. 1 is achievable and also has been demonstrated in Fig. 3 by using 3-D simulation tool based on film-mode matching method (FIMMPROP). In case of launching fundamental TM-mode, the intensity coupling to both of TE and TM modes for port-1 and port-2 is plotted vs. length of HSM as Fig. 4. According to the inset of Fig. 4, the extinction ratio (ER) in case of Fig. 3(a) (length = 1800-μm), defined as $ER(TM_{in}) = 10\log(P_{TE}/P_{TM})_{Port-1}$ is higher than 50dB; meanwhile, the conversion ratio (CR) reaches to 99%. $CR(TM_{in}) = \dfrac{P_{TE(port-1+port-2)}}{P_{TE(port-1+port-2)} + P_{TM(port-1+port-2)}}$

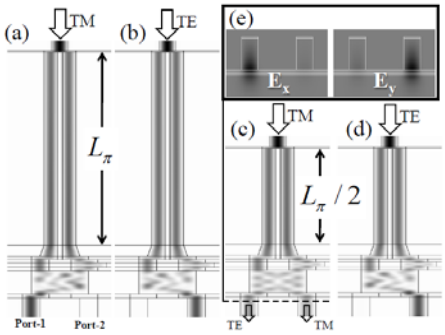

Fig. 3. Simulated intensity map. Length of HSM: (a) (b) L_π, (c) (d) $L_\pi/2$, (e) Cross-section output E-field in case of (c).

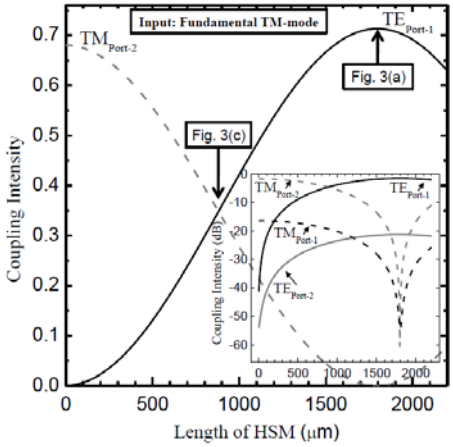

Fig. 4. Coupling intensity vs. length of HSM in case of launching fundamental TM-mode. (Inset: unit in dB)

4. CONCLUSIONS

For integrated PCs, functions of polarization splitting accompanying with polarization conversion from a novel layout based on the unique coupled HSM structure has been demonstrated by simulation. Total device length is less than 2.5mm. In addition, 3dB TE/TM polarization conversion/splitting can be achievable when the length of HSM is $L_\pi/2$ as Fig. 3(c). Moreover, the design only containing vertical shape waveguides without any stepper or angle sidewall will bring many advantages in PICs integration.

ACKNOWLEDGMENT

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DIELECTRIC CONSTANTS WITH EXTENDED MODEL OF INTERBAND TRANSITION CONTRIBUTIONS FOR AlGaInAs QUATERNARY SEMICONDUCTOR ALLOYS

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ABSTRACT

The spectral behavior of the refractive index of AlGaInAs quaternary III-V semiconductor alloy in the energy range from 0.4 to 4eV, including the transparent region, is revisited in order to minimize losses in Bragg reflectors. The extended model of interband transition contributions incorporates not only the fundamental absorption edge contribution to the dielectric function, but also contributions from higher energy and indirect transitions. It is demonstrated that indirect energy transitions must be included in the calculations of the complex dielectric function of the material in the transparent region

1. INTRODUCTION

The design and analysis of such devices as injection lasers, photodiodes, detectors, solar cells, multilayer structures, and microcavities requires the exact knowledge of the optical constants of III-V compound semiconductors in the region near the fundamental absorption edge as well as at the higher photon energies. In modeling of the optical constants of semiconductors in the fundamental optical region, several approaches are typically used: (1) empirical formulas, (2) damped harmonic oscillator (DHO) models, (3) standard critical point (SCP) models. Optical constants determined from empirical formulas (such as the Sellmeier dispersion equations for the refractive index and Urbach's rule for the absorption coefficient [1], or the expression for n based on interpolation of a dielectric quantity using Vegard's rule by Burkhard *et al.*[2]) are not related through the Kramers-Kronig dispersion relation and are valid only over a very limited energy range.

A semi-empirical single effective oscillator model based on quasi-classical Boltzmann equation or Drude theory proposed by Wemple *et al.*[3] does provide an analytical expression for the dispersion of the semiconductor refractive index at photon energies significantly below the direct band edge. This model lacks the agreement with experimental data at the band edge, which is the energy range of the most interest for semiconductor laser devices.

The standard critical point (SCP) model can determine the position of critical points of the semiconductor band structure, but cannot accurately predict the dielectric function [4]. The modified SCP model was initially proposed by Korovin [5] and Cardona *et al.*[6], and then developed by Adachi [7], and Lin *et al.*[8]. The model of interband transition contributions (ITC model) was introduced as a method to analyze the refractive index of III-V compounds at energies below and above the direct band gap by including the electron-hole pair transitions, and by adding the excitonic terms at the two lowest energy gap transitions.

In the present work, an extended model of interband transition contributions (EITC) is developed for the calculations of real and imaginary parts of the dielectric constant of compound semiconductors. The model introduces (1) the broadening effects, caused by phonon and defect scattering in direct and indirect transitions; (2) the strength of direct band gap transitions as a function of the effective electron, heavy hole and light hole masses of the semiconductor; (3) the exciton contributions; (4) the separate contributions of E_x and E_l indirect band gap transitions to the real and imaginary part of the dielectric constant. The importance of indirect and higher direct energy transitions is demonstrated through these calculations and through the comparison with experimental results. The detailed description of our extended ITC model is given in Reference [9], where the index of refraction for the ternary and quatenary alloys has also been calculated and compared with the available experimental results. In this work we apply the extended ITC model for the calculation of the dielectric constant of AlGaInAs alloy, which is then used for the Bragg mirror design.

2. THE EXTENDED ITC MODEL

The dielectric constant $\varepsilon(E) = \varepsilon_1(E)+i\varepsilon_2(E)$ describes the optical response of the medium as a function of photon energy E. The imaginary part of the dielectric function $\varepsilon_2(E)$ is calculated based on a simplified model of the band structure using the joint density of states for each Critical Point (CP) considered. The real part of the dielectric function $\varepsilon_1(E)$ was calculated through the knowledge of the imaginary part, $\varepsilon_2(E)$, by employing the Kramers-Kronig relation. The critical points are associated with electronic transitions in the band structure at the energies designated as E_0, $E_0+\Delta$, E_0^{ex}, E_1, E_2, and E_i. In case of quaternary, $A_xB_yC_zD$,

semiconductor alloy each of the terms become a function of the alloy mole fraction, x, y and z=1-x-y. There are several absorption mechanisms that contribute to the imaginary part of the dielectric constant, therefore $\varepsilon_2(E)$ can be written as:

$$\varepsilon_2(E,x,y)=\varepsilon_2^{Eo}(E,x,y)+\varepsilon_2^{exEo}(E,x,y)+\varepsilon_2^{Eo+\Delta}(E,x,y)+ \\ +\varepsilon_2^{E1}(E,x,y)+\varepsilon_2^{E2}(E,x,y)+\varepsilon_2^{Ei}(E,x,y) \quad (1)$$

where ε_2^{Eo} and $\varepsilon_2^{Eo+\Delta}$ are contributions due to the absorption by direct interband optical transitions near the fundamental absorption edge and spin-orbit transitions, ε_2^{exEo} is due to the absorption by the discrete series of excitons near the E_0 energy gap, ε_2^{E1} and ε_2^{E2} are contributions of the higher energy interband transitions, and ε_2^{Ei} is due to the indirect interband absorption effects. Similarly, the real part of the dielectric function can be presented as the following sum:

$$\varepsilon_1(E,x,y)=\varepsilon_1^{Eo}(E,x,y)+\varepsilon_1^{exEo}(E,x,y)+\varepsilon_1^{Eo+\Delta}(E,x,y)+ \\ +\varepsilon_1^{E1}(E,x,y)+\varepsilon_1^{E2}(E,x,y)+\varepsilon_1^{Ei}(E,x,y) \quad (2)$$

For III-V zinc-blende type semiconductors, the contributions of two main peaks (E_1 and E_2) must also be included. The E_1 peak is treated as a two-dimensional M_0 type critical point, while the structure of the E_2 peak is characteristic of a damped harmonic oscillator.

The detailed description of the individual contributions to the real and imaginary parts of the dielectric constant is given in the Reference [9]. The presented model is applicable in the photon energy range from 0.4eV to about 4eV.

3. CALCULATION RESULTS AND DISCUSSION

The present investigation of the optical properties of the III-V semiconductor alloys is centered on describing the behavior of the refractive index for the photon energies in the transparent region as well as for the higher energies. The calculated index of refraction from our extended ITC model and the available experimental data for AlGaInAs quaternary semiconductor alloy are shown in Fig. 1 demonstrating excellent agreement between the two.

The strongest resonance peak of the index of refraction occurs at the E_1 transition energy.

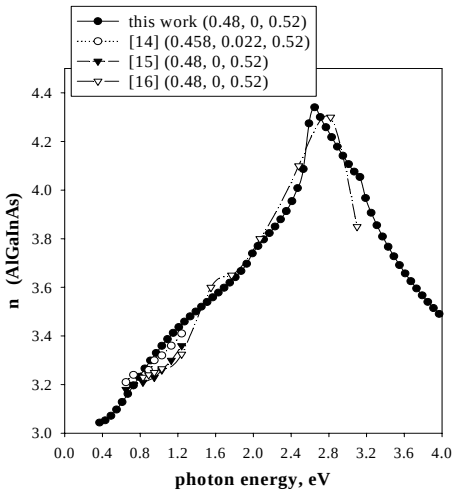

Fig. 1: Refractive index of $Al_xGa_yIn_zAs$ for x=0.48, y=0, z=0.52.

4. SUMMARY

The largest contribution to the dielectric function is due to the direct and indirect optical transitions along <111> and <100> directions in the BZ, which accounts for 85-90% of the total contributions. Therefore, except for the optical absorption in the vicinity of the Γ gap, most of the optical properties of the material, especially the index of refraction, are determined by the electronic structure around L point, rather than at the center of the BZ.

ACKNOWLEDGMENTS

The investigation was funded partially by the University of Maryland Materials Research Science and Engineering Center.

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ELECTRO-OPTICAL ANALYSIS OF THE DEGRADATION OF ADVANCED InGaN-LASER STRUCTURES

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ABSTRACT

Within this paper we analyze the physical mechanisms causing the degradation of InGaN-based Blu-ray laser diodes (LD) and LED structures (with the same epitaxial structure of laser diodes), submitted to stress at 70 °C, 4 kA/cm^2. Data were collected by means of electro-optical measurements, electroluminescence characterization, and near field emission measurements, and provide experimental evidence for the following: *(i)* stress induces an increase in threshold current, according to the square root of stress time, and a decrease in sub-threshold emission; *(ii)* stress induces a slight variation in the slope efficiency of the LDs; *(iii)* during stress the output power of LED samples showed a significant decrease, and *(iv)* the characteristic yellow luminescence signal decreased with a weaker dependence on stress time with respect to the main violet peak.

1. EXPERIMENTAL DETAILS

The study was carried out on InGaN-based devices with a Multi Quantum Well (MQW) structure, emitting at 405 nm. A split-wafer experiment was designed as described in the following: part of the wafer was processed in order to obtain LDs, with cavity width and length equal to 1.5 µm and 600 µm respectively. The remaining part of the wafer was processed in order to obtain LED samples (referred to as LED-like in the following) with the same epitaxial structure of the LDs, and an area of 75 x 200 µm^2. Devices were submitted to constant current stress at 4 kA/cm^2, with a case temperature equal to 75 °C.

2. RESULTS

Optical measurements During stress, the optical power of LED-like devices showed a remarkable decrease, more prominent at lower measuring current levels (Fig. 1). This kinetic indicates an increase in defect density within the active layer, that reduces the radiative recombination rate and consequently the luminescence. Stress was found to induce also an increase in the threshold current (Ith), following the square root of stress time, as reported in previous papers [1]. The slope efficiency showed only a slight decrease, possibly related to an increase in mirror or internal losses, that cannot explain the observed threshold current increase. From the optical power measurement we have calculated the A/Bn ratio (related to the non-radiative recombination rate A) as follows:

$$\frac{1}{\eta}=\frac{I}{P_{out}}=\frac{A+Bn}{Bn}=\frac{A}{Bn}+1 \qquad (1)$$

In (1), η represents the external efficiency, P_{out} is the emitted optical power, A and B are the non-radiative and radiative recombination coefficients respectively. Fig. 2 reports the temporal variations of these values, highlighting a strict correlation between I_{th} and A/Bn.

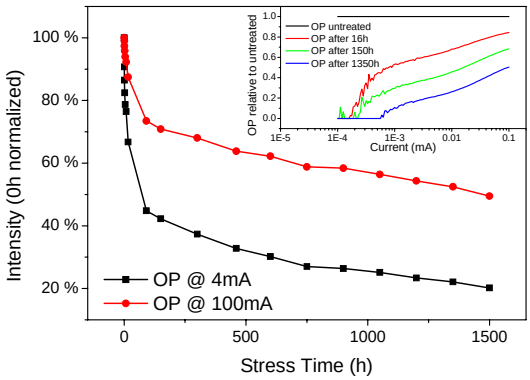

Fig. 1: LED-like optical power measured at 25 °C during stress at 4 kA/cm^2 ,75 °C of a LED-like sample. Inset: normalized L-I characteristics measured during stress time on the same device

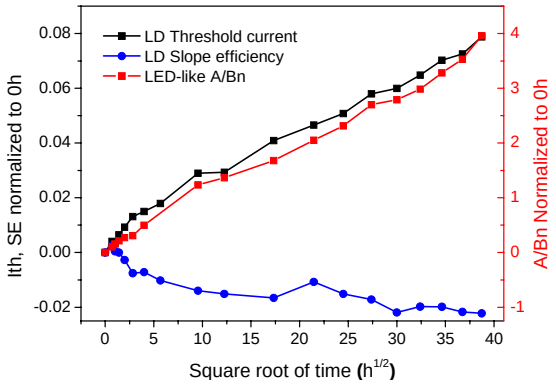

Fig. 2: degradation of the optical parameters of one of the analyzed LDs, submitted to stress at 25 °C, 4 kA/cm^2. Correlation with LED-like A/Bn parameter is also reported

Electrical measurements We have measured the current-voltage curves of the LED-like samples for increasing stress times. Fig. 3 indicates that stress induces an increase in the defect-related current components, which is well correlated with the optical power decrease, thus

suggesting that stress induces an increase in the concentration of defects within the active region [2].

Electroluminescence measurements In order to analyze defect-assisted recombination, we performed spectral measurements to obtain data on the typical yellow luminescence (YL) caused by nitrogen vacancies in the crystal lattice. Fig. 4 displays the results.

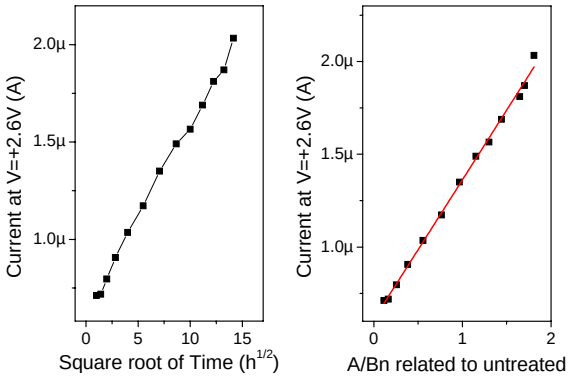

Fig. 3: defect-related current increase and correlation with A/Bn for LED-like structures stressed at 4 kA/cm^2, 75 °C

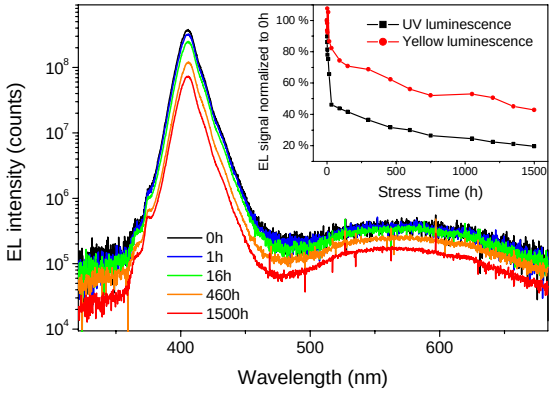

Fig. 4: EL spectra at 25 °C (polarization current = 4mA) and kinetics of LED-like samples after stress at 4 kA/cm^2, 75 °C

The first ageing effect we can notice is the decrement in both the violet and yellow luminescence, and a smaller reduction in the YL (as shown by the inset). Moreover, during stress time no further parasitic emission band was generated. This result confirms that degradation is due non-radiative effects, rather than to the generation of radiative/parasitic emission peaks.

Characteristic Temperature The characteristic temperature (T_0) of the LD was analyzed with the aim of understanding the degradation mechanisms occurring in LDs (see [3]), thanks to the relationship with various parameters

$$\frac{1}{T_0} = \frac{1}{T_{tr}} + \frac{1}{T_{\eta_i}} + \frac{\alpha_i + \alpha_m}{\Gamma_{g_0}} \frac{1}{T_{g_0}} + \frac{\alpha_i}{\alpha_i + \alpha_m} \frac{1}{T_{\alpha_i}} \quad (2)$$

T_0 can be extrapolated from the formula $I_{th} = I_0 e^{T/T0}$, as reported Fig. 5 for increasing stress times. From the reported curves one can notice that the variation with aging consists only in a translation (due to the increase in I_{th} as seen in Fig. 2), with no variation of T_0.

The stability of T_0 during degradation is due to the invariance of LD characteristic parameters (in particular the injection efficiency η_i), at least in the range of temperatures studied within this analysis.

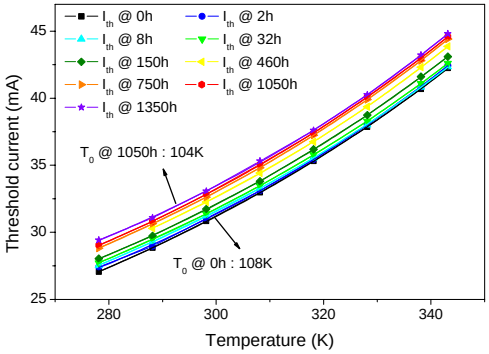

Fig. 5: characteristic temperature fits of LDs during stress at 4 kA/cm^2, 75 °C

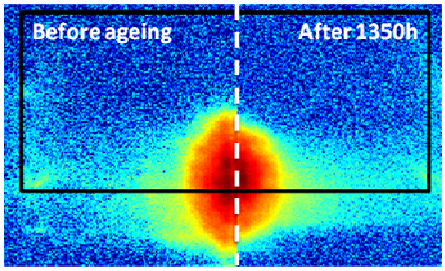

Fig. 6: near field emission microscopy map of one of the analyzed laser diodes, measured at 1mA

Near field emission One of the mechanisms responsible for the decay in optical performances is the current spreading from the active region to the outer parts of the device, causing a worsening of the optical confinement. From Fig. 6 we can infer that no additional spreading becomes visible after stress, while the reduction in spot size is due to the decrease in optical power. This image was taken in near-field imaging, and is presented in logarithmic false-color scale.

3. CONCLUSIONS

The purpose of this work is to describe the mechanisms causing InGaN laser degradation, with specific attention to defect concentration and injection efficiency.

From the experimental data we can deduce that: *(i)* ageing causes an increase in defect density, therefore increasing the non-radiative recombination coefficient and lessening the output optical power; *(ii)* current confinement and injection efficiency do not significantly vary during stress time, causing only a minor decrease in slope efficiency.

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FUNCTIONAL FIANITE FILMS IN PHOTONICS

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ABSTRACT

Fianite has a unique combination of physical properties that made it a very promising material for a wide range of applications in optoelectronics [1, 2]. In this work, we consider the use of fianite as functional films for photonics.

1. INTRODUCTION

The further progress in photonics, as well as in many other technological fields is connected with application of new materials. Fianite is the material of such kind. Industrial technology of synthesis of fianite has been for the first time developed in Russia in the Lebedev Physical Institute of the Russian Academy of Sciences (FIAN in Russian), as has entitled crystals. Serial production of the crystals has been already started in the early seventies of XX century. The volume of manufacture fianite crystals take now the second place in the world after silicon. Fianite single crystals – zirconia-based solid solutions (or "yttrium stabilized zirconia" - YSZ) are widely known worldwide as jewelery material. Recently, in the countries with the developed microelectronics a significant growth of interest to various aspects of fianite application in semiconductor technologies has been observed. Fianite is an extremely promising multipurpose material for new optoelectronics technologies due to its unique combination of physical and chemical properties. It can be used in virtually all of the main technological stages of the production of micro-, opto- and SHF-electronics: as a bulk dielectric substrate and a material for buffer layers in heteroepitaxy; as a material for insulating, antireflection, and protective layers in devices ; and as an gate dielectric. Modern aspects of the application of fianite as functional films in photonics analyzed in this paper.

2. FIANITE AS GATE DIELECTRIC

The use of fianite, as well as ZrO_2 and HfO_2 oxides instead of SiO_2 as gate dielectrics in CMOC technology, which can be considered for microelectronics as a basic one, is of peculiar interest. That is associated with the increase of leakage currents by the increase of integration level when conventional SiO_2 is used. Therefore, a change of SiO_2 over dielectrics with higher values of dielectric constant (high*k*-materials) is required. Due to higher value of dielectric constant (25–30 for fianite against 12 for SiO_2) it is possible to provide the same electric capacity at a higher thickness of the gate oxide. Mirror-flat fianite layers with 10 - 15 nm thickness have been grown on Si substrates by means of laser deposition followed by subsequent re-crystallization annealing. The films have been applied as a ***gate dielectric***. Low value of leakage current was a figure of merit of the layers: 10^{-12} A/cm^2 at 1 V.

3. FUNCTIONAL FIANITE FILMS

The unique properties of fianite as protecting, stabilizing and antireflecting coatings in optoelectronic devices have been demonstrated. Porosity of fianite and ZrO_2 films has been shown to be less than $0.15 \div 0.2$ cm^{-2} , being 1.5-2 order of magnitude lower average values of conventional for SiO_2 films ($4 \div 8$ cm^{-2}). Thus providing the evidence of the advantage of fianite as ***protecting layer*** for electronic and optoelectronic devices.

4. ANTIREFLECTION FIANITE COATING

Excellent prospects for application of fianite as an ***antireflection coating*** for Ge, Si and $A^{III}B^{V}$ devices have been demonstrated both theoretically and experimentally. Films that cover the working surface of a photodetector (PD) must possess not only the protective and stabilizing properties needed for microelectronic devices but antireflection

properties as well, since reflection losses R would be considerable without such a coating. For example, the optical refraction factor n=3.7 for Si; 4 for Ge. Therefore, R_{Si} =43%, R_{Ge}=40%. The high transparency of fianite over a wide spectral range (0.25–7.5 μm) allows its use in photoreceptors (PRs) that operate in the wide spectral range of UV to middle_IR. Fianite can be used to make windows for wide_gap PRs used, e.g., in focal plane arrays that simultaneously record laser radiation with a wavelength of 1.54 μm and thermal radiation with wavelengths of 3–5 μm. A dielectric with a refraction factor of nd = ~ 2 (if n = 3.7–4) is optimal for making an antireflection coating. Having a thickness of one_quarter of the optical wavelength, $W = \lambda/4nd$, such a dielectric theoretically eliminates all reflective loss (R = 0). The refraction factor of SiO_2 (n = 1.47) is considerably less than the optimal value. With such an n, the reflective loss cannot be reduced to below 10%. The refractive factors of fianite (2.15–2.18) and ZrO_2 (2.13–2.2) are close to the mentioned optimum value. Fianite and ZrO_2 are therefore better than SiO_2 as antireflection coatings.

Modes of deposition of the ***antireflecting fianite films*** on InGaAsP/GaAs multilayer structures by means of magnetron sputtering have been developed. It has been experimentally established that the use of fianite antireflecting coatings in Ge and Si photodiodes allowed achieving zero reflection loss. Fianite protective films totally eliminated excess of noise in Ge photodiodes. Application of fianite protective coatings permitted manufacturing of multielements Ge code photodiode with improved photoelectric characteristics and increased reliability. Model samples of Ge photodiodes with fianite protective and stabilizing layers have been produced. Application of fianite protective coatings in Ge photodiodes eliminated shot noise, thus, in principle improving photoelectric characteristics.

Solar cells with multilayer InGaAsP heterostructures on InP and GaAs substrates with/and /without fianite antireflection coverings have been compared. It has been established that the efficiency of solar cell with fianite-coating was 20% higher than that of solar cell without antireflection coating.

Technologies of opto-electronic devices based on the "semiconductor-fianite" structures have been developed. Three types of photodetectors based on the "semiconductor-fianite" structures have been designed, produced and studied: germanium code photodiode (PD); laser photodiode (PD); high-sensitive IR multielement photodetector (IR-MPD).

5. PROPERTIES OF DEVICE STRUCTURES WITH FIANITE AND ZrO_2 FILMS

The photovoltaic characteristics and noise of two types of germanium photodiodes were studied earlier: ones with fianite and ZrO_2 films, and ones with SiO_2 films. The monochromatic sensitivity of these devices was typical of germanium instruments and had a value of 0.5–0.6 A W^{-1} (at wavelengths of 1.06 and 1.55 μm). Replacing the SiO_2 oxide with ZrO_2 oxide or fianite led to a slight reduction in dark current (on average, by 10%). The fundamental improvement in photodiode properties due to the fianite or ZrO_2 film became apparent in noise studies. In what amounted to an accelerated reliability test, control samples with SiO_2 films showed a telegraph like pulse noise on oscillograms at voltages higher than the operating voltage; this may have been due to surface conducting channels switching on and off. Defects caused by the pores in SiO_2 oxide could be the reason for the appearance of surface channels. Only shot noise (basically unavoidable) was observed in the samples with fianite or ZrO_2 protective coating.

Results obtained in this work have actually demonstrated advantages of fianite as novel multipurpose material for new optoelectronics technologies.

ACKNOWLEDGEMENTS

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Session 11 :

Miscellaneous : novel materials, devices and applications

Chair : Prof. David Pulfrey

Wednesday June 1, 14:30 - 16:10

RESONANT MEMS WITH TWO-DIMENSIONAL ELECTRON GAS SYSTEM

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ABSTRACT

In the paper we develop a model accounting for the influence of the electric field fringing on the output source-drain current in the 2DEG channel of the high-electron mobility transistor (HEMT)-based resonant MEMS with micromachined cantilever serving as a floating gate.

1. INTRODUCTION

Operation of mass sensors with resonating micro/nano cantilevers is based on the measurement of the shift of cantilever' s resonant frequency associated with the change of its mass due to loading of the molecules of the substance to be detected. Usually frequency shift is measured by means of optical or capacitive readout techniques. For multi-target detection the arrays of the cantilevers are used. The increase in the number of cantilevers is inevitably accompanied by increasing complexity of the readout system. Electrical readout when mechanical oscillations of the cantilever are transduced directly into output electric signal seems to be very promising.

Resonant gate transistor [1] has been the first MEMS with electrical readout in which current flowing in the transistor channel has been controlled by micromachined gate. Recently resonant gate transistor concept has been extended to high-electron mobility transistor (HEMT) with cantilever playing the role of the floating gate [2]. Incorporation of cantilever arrays in such HEMT-based resonant sensors [3] has been proposed to expand their application range to multi-target detection as well as to enhance the output signal. In the existing analytical models the cantilever - two-dimensional electron gas (2DEG) system is usually represented by an ideal capacitance and impact of the electric field fringing is neglected. In this paper we develop realistic model for the HEMT-based resonant MEMS.

2. MODEL AND SHEET ELECTRON DENSITY DISTRIBUTION IN THE 2DEG CHANNEL

We consider a structure schematically shown in Fig.1 with 2DEG channel formed at the AlGaAs/GaAs heterointerface. The channel is supplied with source and drain contacts. Micromachined cantilever plays the role of a floating gate. Source-drain current can be controlled by bias voltage $V_c(t)=V_0+\delta V_\omega \exp(j\omega t)$ applied to the cantilever, where V_0 and δV_ω are dc and ac amplitudes, respectively. ac signal excites the vibrations of the cantilever causing the variation of the electric field at 2DEG channel surface which results in the variation of electron concentration in the channel, its resistance and source-drain current. When ac signal frequency ω coincides with the resonant frequency of cantilever's mechanical oscillations source-drain current reveals a peak. Shift in the resonant frequency can be registered as the shift of the current peak.

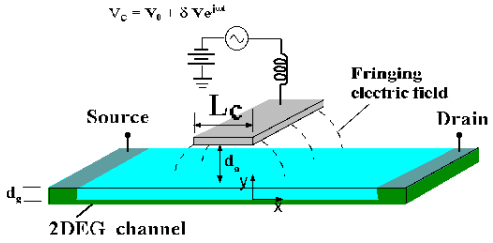

Fig.1:. Schematic structure of HEMT-based resonant MEMS with micromachined cantilever .

Usually the cantilever - 2DEG system is represented by two ideal capacitors connected in series. However air gap d_a between the cantilever and top surface of the semiconductor structure is not small and fringing of the electric fields takes place and can affect the output source-drain current. Such an effect may become significant with the scaling down of the cantilever length L_c and/or in the case of multiple cantilevers with small separation between them. To account for fringing effects we derive electric field distribution at 2DEG surface and coordinate x in parametric form [4]:

$$E_{2DEG} = \frac{V_c(t)}{\left[d_g + \varepsilon_r d_a \left(1 - y(t)\right)\right]\left(1 + e^{\xi}\right)}, \qquad (1)$$

$$x = \frac{d}{\pi}\left(1 + \xi + e^{\xi}\right), \qquad (2)$$

where ξ is a parameter, d_g and ε_r are the thickness and dielectric constant of the top wide-gap semiconductor layer, $d = d_a + d_g/\varepsilon_r$, $y(t)$ is time-dependent displacement of the cantilever obtained from the solution of the equation of forced damped harmonic oscillations of the cantilever represented as a point mass. Reference point $x=0$ coincides with the edge of the cantilever as shown in Fig.1.

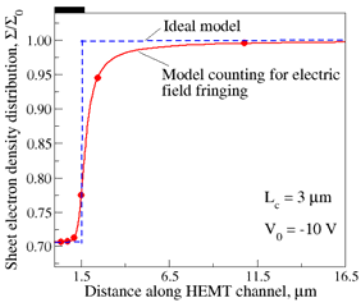

Fig.2: Normalized sheet electron density distribution along 2DEG channel without (dashed line) and with (solid line, filled circles) fringing.

Normalized sheet electron density distribution along 2DEG channel shown in Fig.2 has been calculated using the following formula (which accounts for fringing effects)

$$\frac{\Sigma}{\Sigma_0} = 1 + \frac{\varepsilon_0 \varepsilon_r}{e\Sigma_0} \frac{V_c(t)}{\left[d_g + \varepsilon_r d_a (1 - y(t))\right]\left(1 + e^{\xi}\right)}, \qquad (3)$$

where e is the electron charge and Σ_0 is initial sheet electron density in the channel. Comparing distributions of Fig.2 obtained with ideal and developed fringed models one can see that electric field fringing affects not only the "ungated" portions of the 2DEG channel but the region beneath the cantilever as well. Although the present model is developed for a single cantilever one can estimate from Fig.2 that in the case of multiple cantilevers the reduction in the separation between them will result in deviation of sheet electron density in the "ungated" regions from initial one.

3. CALCULATION OF THE SOURCE-DRAIN CURRENT

Due to nonuniform distribution of the sheet electron density along 2DEG channel its resistance occurs to be distributed: $dR_{2DEG}(x) = dx/\Sigma(x)$ and to find it one needs to integrate. Using Eq.(2) and changing the variable x to ξ we finally arrive at

$$R_{2DEG} = \frac{2d}{\pi e \mu W \Sigma_0} \int_{\xi_l}^{\xi_r} \frac{\left(1 + e^{\xi}\right)^2 d\xi}{\left[1 + e^{\xi} + v(t)\right]}, \qquad (4)$$

Where $v(t) = \varepsilon_0 \varepsilon_r V_c(t)/ed\Sigma_0$, $\xi_r = \xi(x=L_{un})$ and $\xi_l = \xi(x= -L_c/2)$. 2DEG channel resistance and the source-drain current can be represented as $R_{2DEG} = R_0 + \delta R_\omega exp(j\omega t)$ and $I_{sd} = V_{sd}/R_{2DEG} = I_{sd}^0 + \delta I_\omega exp(j\omega t)$, respectively. Substituting Eq.(4) into expression for the source-drain current I_{sd} and expanding the latter under the assumption that $\delta V_\omega << V_0$ and $\delta I_\omega << I_{sd}^0$ we obtained

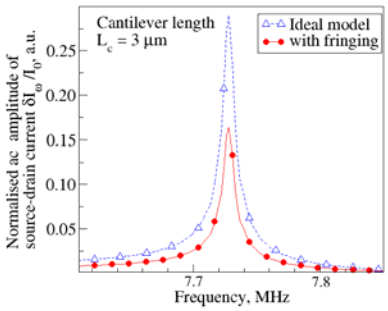

Fig.3: Frequency dependence of normalized amplitude of the ac component of the source-drain current without (dashed line with triangles) and with (solid line with circles) fringing.

the expression for the modulus of normalized ac amplitude of the source-drain current $|\delta I_\omega / I_{sd}^0|$. Frequency dependence of normalized amplitude $|\delta I_\omega / I_{sd}^0|$ is shown in Fig.3 (solid line with circles). One can see from Fig.3 that electric field fringing results in the reduction of the peak amplitude of the source-drain current at resonant frequency comparing to that obtained with the ideal model (dashed line with triangles).

4. CONCLUSIONS

Simple model which allows to evaluate electric field fringing effect on spatial distribution of the sheet electron density in the 2DEG channel of the resonant MEMS with the HEMT-like structure is developed. The advantage of HEMT-based resonant MEMS is related to the electrical readout realized in such a structure. The frequency-dependent amplitude of the source-drain current is also calculated in the presence of fringing.

The proposed model can be applied for evaluation of multi-cantilever resonant HEMT-based MEMS if separation between cantilevers is large enough. The reduction in cantilevers' spacing requires proper modification of the model.

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MBE GROWN SELF-CATALYZED III-V NANOWIRES ON SILICON

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ABSTRACT

We present recent results on the growth of GaAs nanowires (NW) on Si (111) substrate using molecular beam epitaxy (MBE). The NWs are vertically-aligned and grown without the use of external catalyst material. Structural analysis with high-resolution transmission electron microscopy (HR-TEM) indicates that multiple growth modes are possible on different crystal faces of the NW. Photoluminescence has been used to characterize the optical properties. Additionally, we have attempted to incorporate nitrogen in the NW structure, forming the dilute nitride GaAsN.

1. INTRODUCTION

The dilute nitride materials system represents an important class of semiconductors. Incorporation of several percent nitrogen into III-V alloys such as GaAs results in a large reduction in the bandage and lattice constant[1]. These highly-mismatched alloys, named because of the large difference in both electronegativity and atomic radius between As and N, are of considerable research importance. The ability to control the band gap by varying the amount of nitrogen in the alloy has resulted in applications in optoelectronic and novel photovoltaic materials [2].

Recently, GaAs nanowires have been grown with molecular beam epitaxy (MBE) without the use of an external seed particle, using gallium to catalyze the wire growth[3]. These catalyst-free GaAs nanowires can be grown on a number of substrates, including silicon (111)[4]. Varying the growth conditions allows for control over the physical dimensions of the wires and other elements can be introduced during the growth process, forming core-shell nanowires[5]. In this work we describe the catalyst free growth of GaAs nanowires and GaAs/GaAsN core-shell structure using MBE.

2. EXPERIMENTAL METHODS

Growth was performed with Intervac Gen II MBE with solid source Ga and As, ion- and cryo- pumps, as well as a reflection high-energy electron diffraction (RHEED) system. A DC nitrogen plasma source was used, which has the potential to provide high nitrogen incorporation efficiency, growth stability, and reproducibility [6]. All growths were performed on Si (111) substrate with the native-oxide layer left intact before growth. The substrate was heated to 580C and the exposed to Ga flux for 5 seconds, allowing for the formation of Ga droplets on the surface. The As flux was then turned on and GaAs wires were grown.

To grow GaAs/GaAsN core-shell structure, GaAs NW's were first grown, followed by growth interruption, during which the N plasma source was ignited and the substrate temperature was dropped. The Ga shutter was then reopened and GaAsN was grown layer was grown.

The size, shape, and areal density of the samples were characterized with scanning electron microscopy (SEM) and the composition and crystallinity were investigated with hi-resolution X-ray diffraction (XRD), using a Phillips X'pert Pro X-ray diffractometer. Optical properties of nanowires were investigated using low-temperature micro-photoluminescence (PL).

3. RESULTS AND DISCUSSION

3.1. Scanning electron microscopy

Fig. 1(a) shows a typical SEM image of GaAs NW's grown on Si (111) substrate. GaAs/GaAsN core-shell NW structure is shown in Fig. 1(b). The NW's are vertically oriented and of uniform areal density.

3.2. X-ray diffraction

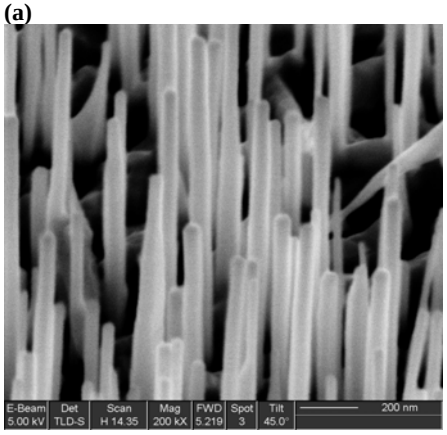
XRD of the GaAs sample shows the GaAs zinc-blende (111) GaAs peak, confirming crystallinity of the sample, in addition to peaks form the Si (111) substrate.

3.3 Photoluminescence

In order to isolate the effect of an individual wire, micro-PL was performed on NW after mechanical transfer to a clean Si(111) substrate. GaAs NW exhibit sharp low-temperature PL as shown in Fig 2(c). The luminescence peak at 1.52 eV agrees with results obtained in other works. The intensity of the PL peak as function of excitation power is plotted in Fig. 2(c) inset, displaying a linear dependence, indicating a single-photon process.

Micro-PL of GaAs/GaAsN core-shell structure is displayed in Fig. 2(d). The luminescence peak is considerably broadened, due perhaps do perhaps to the poor quality of the GaAsN layer or lack of a cladding layer. A shift in luminescence peak to lower energy is observed, consistent with the incorporation of nitrogen. Also observed are sharp lines in the GaAsN photoluminescence, which have been reported before as arising from the recombination of carriers through localized and delocalized states[7].

(a)



(b)

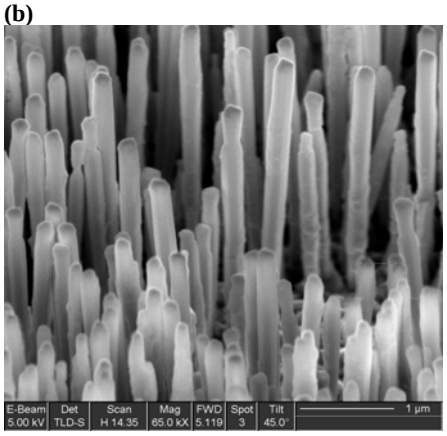


Fig. 1: (a) SEM image of GaAs NW's grown on Si (111) substrate. (b) SEM image of GaAs/GaAsN core-shell NW structure.

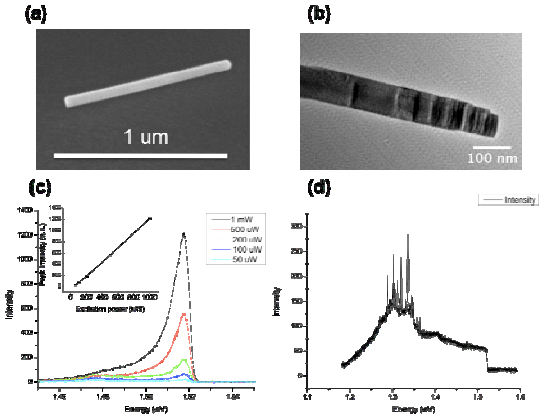


Fig. 2: (a) SEM image of GaAs NW after mechanical transfer to Si (111) substrate. (b) TEM image of GaAs NW. (c) Micro-PL spectra of GaAs NW at 4K, the inset shows the dependence of peak intensity on excitation power. (d) PL spectra of GaAs/GaAsN core-shell NW at 4K. A luminescence peak at 1.31 eV corresponds to 0.7% N incorporation.

4. CONCLUSION

We present preliminary results on the growth and characterization of GaAs NW's and GaAs/GaAsN core-shell structure. GaAs NW's display sharp PL linewidth. The addition of a GaAsN shell layer results in a redshift in the luminescence peak and degraded optical properties, suggesting that growth conditions need further optimization. Further efforts to investigate the composition and structure of the NW's using transmission electron microscopy (TEM) are underway.

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HIGH MOBILITY n-TYPE Zn_3N_2 THIN FILMS AS CHANNEL FOR THIN FILM TRANSISTORS

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ABSTRACT

Zn_3N_2 films were grown by rf-magnetron sputtering in Ar/N_2 ambient using Zn target (99.995%) on glass substrates. Electrical properties such as resistivity, mobility, and carrier concentration were determined by Hall-effect measurements using the four-probe Van der Pauw technique. Through the optimization of the growth conditions, a maximum mobility of 99 cm^2/Vs was achieved for an electron concentration of 3.2×10^{18} cm^{-3} at a 423-K growth temperature, 4.4-nm/min growth rate, and 73%-rich N_2 ambient. Resistivity varied from 1.2×10^{-3} to 5×10^{-2} Ω cm as a function of the growth conditions. TFTs were successfully fabricated using those layers as a channel. I_D/V_{DS} output characteristics were analyzed and resultant field effect mobility around 0.06 cm^2/Vs was calculated.

1. INTRODUCTION

Thin film transistors (TFTs) are essential devices in active-matrix liquid crystal and organic light-emitting diode displays. Although hydrogenated amorphous silicon is usually the material of choice for the TFT channel, this technology presents some issues such as the low mobility or the poor levels of stability (Figure 1(a)). Therefore, different organic and inorganic materials are being investigated as potential substitutes. One of them is zinc nitride (Zn_3N_2), which is attractive due to its high mobility (Figure 1(b)) and conductivity as well as its low-cost processing. Electrical characteristics of Zn_3N_2 films grown by rf-magnetron sputtering were thoroughly studied in previous works [1]. Moreover, Zn_3N_2 was recently used in a TFT structure as channel [2] although the device only exhibited transistor characteristics after an annealing process.

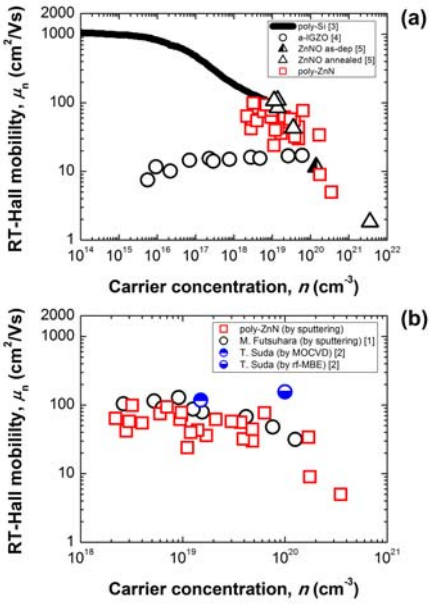

Fig. 1: μ as a function of n for (a) different materials and for (b) Zn_3N_2 grown by different techniques. Resultant μ values for this work were also represented (red squares) for the sake of comparison.

In order to optimize the output characteristics of TFT devices, this work aims to improve the electrical properties of Zn_3N_2 layers grown by rf-magnetron sputtering through the optimization of the growth conditions and the fabrication of top-gate TFTs using as-deposited Zn_3N_2 as channel.

2. EXPERIMENTAL

Those layers were synthesized by radio-frequency magnetron sputtering from a pure Zn (99.995% purity) target using a mixture of N_2 (99.999% purity) and Ar (99.995% purity) as working gases. Each gas was introduced through their own mass controller so total gas flux can be easily controlled. Deposition parameters were varied in order to establish different growth rates (3.8 - 73.3 nm/min) and layer thicknesses (0.1 - 2.2 μm) as measured with a stylus profiler. Prior to deposition, glass substrates were rinsed using ethanol, acetone, and sputter cleaned with N_2 to avoid unintentional surface impurities; additionally, the target was also sputtered during 5 min.

Stoichiometry and thicknesses of Zn_3N_2 layers were determined by RBS measurements performed at the Center of Microanalysis of Materials (CMAM/UAM) after SIMNRA analysis. Samples were irradiated with two different He^{2+} beam energies: 3.7 and 3.045 MeV; those energies enhanced the backscattered signal from N and O atoms, respectively.

Surface morphology of the Zn_3N_2 samples was examined by means of scanning electron microscopy (SEM, Philips XL 30 S). Their crystal structure was investigated by X-ray diffraction (XRD, Siemens D-5000) with Cu-K_α1 radiation at the interdepartmental research service (SIDI-UAM).

Electrical properties such as resistivity (ρ), mobility (μ_n), and carrier concentration (n) were determined by

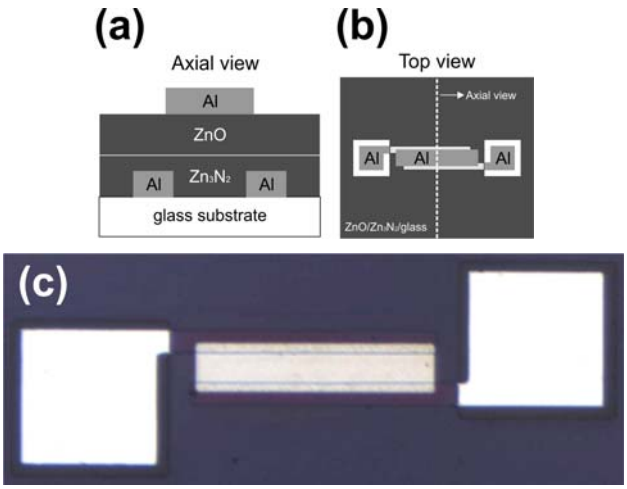

Fig. 2: Top-gate Zn_3N_2 TFT fabricated. Axial (a) and top view (b) of the TFT design. (c) Resultant TFT image.

room-temperature Hall-Effect measurements using the four-probe Van der Pauw technique.

Figure 2 shows a schematic of the top-gate Zn_3N_2 TFT fabricated. Evaporated and patterned 200-nm thick Al on glass substrates was used as a drain and source electrodes. The conductive channel consisted of a Zn_3N_2 layer grown by rf-magnetron sputtering. The growth parameters were: 423-K growth temperature, 4.4-nm/min growth rate, and 73%-rich N_2 ambient. An insulating 150-nm thick ZnO layer atop Zn_3N_2 layer was deposited by rf-magnetron sputtering in order to prevent surface oxidation and to act as gate insulator. The gate insulator and the channel layer were both chemically etched to open windows on the source and drain contacts. Finally, the gate electrode was defined by optical lithography and lift-off on the ZnO layer. The characteristic I_D/V_{DS} curves for different V_{GS} in dark and light conditions were performed in a four-probe system (Karl Suss Probe Station).

3. RESULTS AND DISCUSSION

3.1. Characterization of zinc nitride films

Scanning electron microscopy (SEM) showed a polycrystalline structure with different grain sizes depending on the deposition temperature (T_s). The increases of the grain size improve the conductivity as Hall measurements confirmed.

The structural properties of the Zn_3N_2 films were analyzed using X-ray diffraction technique between 10 and 90 degrees. The pattern showed only Zn_3N_2 peaks as is recorded in the JCPDS document (Powder Diffraction File Compiled by the Joint Committee on Powder Diffraction, 1985, Card No. 35-0762). SEM shows polycrystalline structures with increasing disorientation as T_s increases.

RBS analysis showed that the composition of Zn_xN_y films grown at different temperatures, had a stoichiometry near x = 3 and y = 2.

Through the optimization of the growth conditions [3], a maximum mobility of 99 cm^2/Vs was achieved for an electron concentration of $3.2x10^{18}$ cm^{-3} at a 423-K growth temperature, 4.4-nm/min growth rate, and 73%-rich N_2 ambient (Figure 1, red squares).

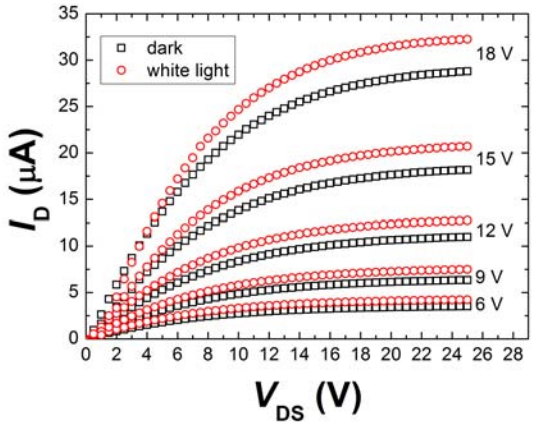

Fig. 3: TFT output characteristics (I_D/V_{DS}) in dark (black squares) and light (red circles) conditions.

3.2. TFT characterization

Resultant TFTs had a channel width W = 180 μm and channel length-to-width ratios W/L = 11.3, 22.5, 45, and 90 defined by separation between patterned Al source/drain electrodes. TFT design gave output characteristics I_D/V_{DS} just after the fabrication which were shown in Figure 3. The transistor was normally off and it required at least 6 V gate voltage (V_G) for the channel to start conducting. The saturation current at that V_G was below 5 μA and increased its value from 5 to 30 μA as V_G increases from 6 to 18 V. Visible light illumination produced high photocurrent levels which increased with V_G significantly. The photosensitivity of the TFT (I_{light}-I_{dark}) was calculated as a function of the V_{GS} in the saturated region (V_D = 20 V) yielding a $(V_{GS}+3)^2$ dependence.

4. CONCLUSIONS

TFTs were successfully fabricated using Zn_3N_2 as channel. Those layers were grown by rf-magnetron sputtering at different growth conditions in order to optimize resultant electrical properties. Maximum layer mobility around 99 cm^2/Vs was achieved at a 423-K T_s and a 4.44-nm/min growth rate. I_D/V_{DS} output characteristics were analyzed obtaining field effect mobility around 0.06 cm^2/V. In addition, it was observed that I_D increases under visible light illumination, that effect increasing with V_G.

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LOW DOSE MICROSCOPY OF SEMICONDUCTING AND METALLIC NANOSTRUCTURES: TOWARDS RECOVERING ORIGINAL MATERIAL STRUCTURES

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ABSTRACT

Aberration-corrected transmission electron microscopy (TEM) with its sub-Ångstrom resolution and enhanced signal-to-noise ratio facilitated new materials investigations. However, electron beam – sample interactions currently limit many observations of nanostructures which are due to their small dimensions often more prone to beam-sample interactions. In this presentation it will be shown how the electron beam affects materials and how this can be suppressed by the use of low dose and low voltage microscopy. First results confirm that low dose microscopy results in signal recovery and in the imaging of additional structures which are invisible under commonly used illumination conditions.

1. INTRODUCTION

Aberration-corrected TEM as well as the development of monochromators and high brightness guns have advanced transmission electron microscopy to a point where resolution is no longer a limiting process in imaging atomic structures[1]. Instead, adequate sample preparation and electron beam-induced material changes have become the center of our attention. It was demonstrated before that atomically clean surfaces are essential for a meaningful interpretation of InGaN epilayers and quantum well structures which in the Ga-rich (In,Ga)N system can be achieved by a final chemical etch[2]. Recently, an FIB-based sample preparation method has been developed which is more generally applicable as it does not rely on chemical etching but focuses on low voltage ion milling[3]. With such clean electron transparent samples TEM imaging is no longer plagued by sample preparation induced defects and ultrahigh resolution TEM is used to discover original material structures.

Recently it was found that phonon-induced atom vibrations significantly change the image of a rhodium nano-cluster under electron beam illumination[4]. A characteristic intensity fluctuation could be described by this phenomenon. Following, beam-induced effects will be described along with a methodical approach to suppress these effects, utilizing low voltage, low dose microscopy.

2. EXPERIMENTAL METHODS

Transmission electron microscopy (TEM) was performed in a TEAM0.5 microscope from FEI which can be operated between 20kV and 300kV acceleration voltage. The instrument features C_S correction (with C_S = -15µm at 80kV) and utilizes a monochromated high brightness (XFEG) beam. Sample preparation varies: Rh nanoclusters on alumina flakes were transported onto a holey carbon grid, nanoneedles were prepared according to Ref. 3 and InGaN cross sectional samples were prepared with a final chemical etch[2].

3. RESULTS AND DISCUSSION

3.1. Image changes in-situ TEM (at 300kV): The case of InN / In_2O_3

In a transmission electron microscope many materials are known to interact at high voltages with the electron beam; displacement damage and phase transformations are two examples. At the surface of an InN epilayer prepared in cross section the formation of In_2O_3 was observed in-situ TEM (at 300kV). Fig. 1 shows the final layer which could be imaged in atomic resolution and demonstrates the TEAM0.5 typical high sensitivity which allows to image low Z elements such as oxygen in direct vicinity of a high mass element such as indium. Nevertheless, such beam sample interactions are unwanted and need to be suppressed.

Fig. 2 shows the probability of knock-on damage characterized by the total cross section for displacement as calculated after Ref. 5. Clearly, atom displacement has to be taken into account if acceleration voltages exceed 20kV, which is most pronounced if the observed material is only a few atomic layers thick. It can also be seen that indium nano-cluster presence is difficult to confirm in TEM images for acceleration voltages above 50kV as atom displacement will be pronounced.

The TEAM0.5 microscope with a resolution of under 1Å for 50kV instrument operation provides a unique

ability to suppress such effects. For light elements such as nitrogen and oxygen a combined atomic resolution and completely suppressed displacement damage are at present not achievable.

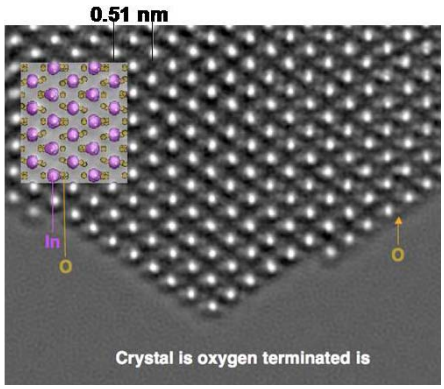

Fig. 1: In_2O_3 [011], formed in-situ at 300kV at the edge of a InN TEM sample. Displayed is the phase of the reconstructed wave function, bright areas correspond to indium columns and atoms. For comparison, the theoretical crystal configuration is shown in the inset.

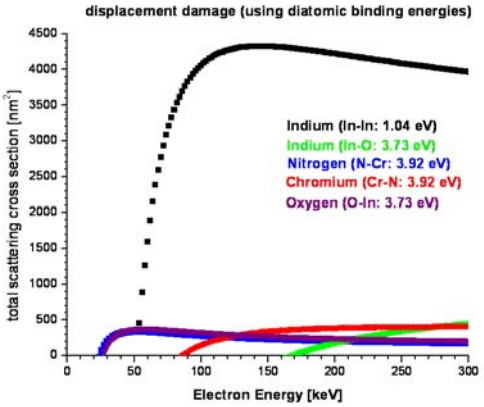

Fig. 2: Atom displacements dependent on the acceleration voltage in a TEM for the case of indiumoxide and CrN. Light elements show no displacement damage only if imaged at very low acceleration voltages around 20 kV.

3.2. Low Dose Microscopy

Another beam-sample interaction which is omnipresent at common TEM operation conditions is the formation of phonons or 3D atom vibrations. This phenomenon was recently found to be responsible for intensity fluctuations which were observed in numerous TEM analyses by microscopy groups all over the world. The typical intensity fluctuations caused by beam-induced phonons could be approximated in a 3D simulation[4]. In order to minimize such effects the electron dose rate needs to be reduced to values which are similar to those recommended for imaging of biological substances.

Fig. 3 shows four images of an industry-style catalyst system, a rhodium crystal oriented in [110] on alumina. In figs. (a) and (c) an electron dose of 5000 $e^-/(Å^2\ s)$ was used, in figs. (b) and (d) only 75 $e^-/(Å^2\ s)$. The top images are single, structural images, the signal-to-noise ratio in fig. 3c is large and only little structure can be seen. However, if one reconstructs a focal series, using up to 100 images with varied focus, the phase of the resulting wave function shows great detail when low dose microscopy is applied. Even atoms at the surface of the crystal become visible when phonon excitation is suppressed while in high dose the reconstructed image does not show those surface features.

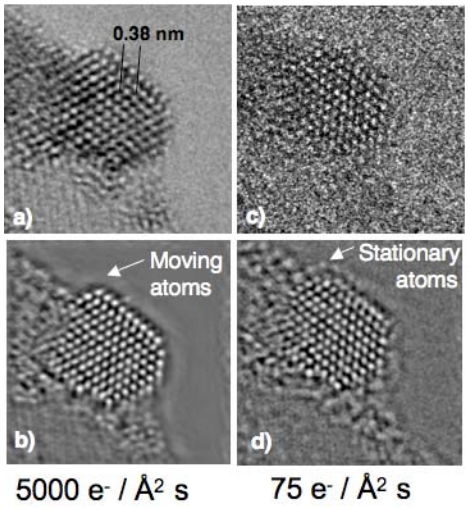

Fig. 3: Example for control of beam-induced phonon excitations by dose variations: Images of a Rh [110] particle on alumina, acceleration voltage: 80kV (a) single image in high dose (b) focal series reconstruction of high dose images (c,d) respective images in low dose

4. CONCLUSION

Different effects of beam-induced material changes in a TEM are discussed. First results of low dose, low voltage microscopy demonstrate imaging of surface structures in great detail due to control of phonon excitation and suppressed displacement damage.

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INTERDIGIT 4H-SIC VERTICAL SCHOTTKY DIODE FOR BETA-VOLTAIC APPLICATIONS

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ABSTRACT

We demonstrated a 4H-SiC vertical Schottky diode for β-voltaic application using an interdigit front metallization. A relevant increase of β-voltaic short circuit current with respect to a device with a continuous standard front electrode was achieved with this novel layout allowing to collect also low energy electrons. By irradiating the device with monochromatic e-beam of 17 keV, an internal Gain 1.4 times higher than in conventional devices was obtained. Open Circuit Voltage of ~ 1 V was obtained for an illumination e-beam current density of 10^{-8} A/cm^2.

1. INTRODUCTION

Power suppliers operating at modest power levels but over long periods (20 years) are required in harsh environments or low-accessibility location applications. Soft β-sources are suitable candidates for these applications [1].

In recent years, wide band gap based devices were considered for their very low leakage current. Among the wide band gap semiconductors, 4H-SiC is the one having the highest maturity for electronic device fabrication. Furthermore, the radiation hardness of SiC ensures the long term stability of a cell.

4H-SiC p-n junctions and Schottky diodes, using standard continuous front electrodes, were previously tested with promising performances for β-voltaic cells fabrication. The use of Schottky barrier can lead to significant simplification of the fabrication process and to a reduction of the manufacturing costs [1], [2]. In this perspective, we propose the use of an interdigit vertical 4H-SiC Schottky diode for β-voltaic applications. In this configuration even lower β energies can be used open to the application of soft emission sources.

2. EXPERIMENTAL DETAILS

Schottky-type devices were fabricated by ST*Microelectronics*-on *n*-type 4*H*-SiC epitaxial layers, 4 μm thick with a residual dopant concentration of *1-3x10^{14} cm^{-3}*, grown by CREE Inc., onto a n-type heavily doped substrate. A large area Ohmic contact on the sample backside was formed by evaporation of a *200 nm* Ni film, followed by a rapid thermal process at *1000 °C*. Schottky contacts were fabricated on the wafer front side by defining the nickel silicide (Ni_2Si) interdigit structures. The devices had a square geometry with a total area *1.2×1.2 mm^2*. The distance between contiguous Ni_2Si stripes in the interdigit front electrode of the devices examined in this paper was *7 μm* or *10 μm*, while the stripes width was *3 μm*. The resulting directly exposed area was of about *65%* and *71%* of the total device area and the samples are identified as *#65* and *#71*, respectively. Further fabrication details are reported in ref. [3], [4].

In order to study the charge collection of the interdigit Schottky diode under electron irradiation, the devices were placed in the e-Line™ chamber of Raith Inc. GmBh.

Current-voltage (*I-V)* characteristics were measured using a Keithley 236 Source Measure Unit (SMU) and a Keithley 428 current amplifier with an internal gain fixed at 10^6. The voltage signal, versus the time, is acquired by the oscilloscope Tektronix TDS 5104.

3. RESULTS AND DISCUSSION

By means of Electron Beam Induced Current (EBIC) measurements, the potential advantages of an interdigit layout for β-voltaic cells with respect to the conventional front electrode is clearly demonstrated. The direct exposure to the β-radiation of the active area in the interdigit 4H-SiC diode reduces the backscattering yield of incident particles with respect to a similar device with continuous electrode. The EBIC measurement was carried out during a "line scan" in direction orthogonal to the metal stripes of the front electrode. Using the X-Y signals from the pattern generator of the e-Line™ system, the plot of the current versus the position along the scanning direction was reconstructed.

In Fig.1 the *17 keV* energy e-beam induced currents, collected at *0 V*, for samples *#65* and *#71*, are plotted as a function of the position along the scanning line. Similar trend of the collected current is obtained in both samples independently of the front electrode geometry. A constant current is obtained in correspondence of the metal stripes irradiation due to the total overlap of the junction depleted region and the charge generation region. Moving the beam outside the metal stripes, we observe a relevant increase of the current due to the lower backscattering yield of SiC with respect to the one of the Ni_2Si [5].

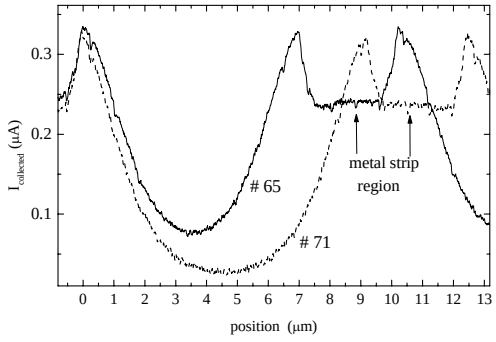

Fig. 1: Collected current as a function of the scan position along a direction orthogonal to the front electrode metal stripes. The e-beam energy is *17 keV*, samples *#65* and *#71* are at *0 V* bias.

A rapid reduction of the current is observed moving the e-beam far from the electrode edge. The plot of Fig. 1 demonstrates that an opportunely designed interdigit device will provide a higher external current with respect to a device with a continuous metal front electrode. In fact, the current obtained irradiating the semiconductor junction region directly exposed is higher than that obtained when the electrons impinge on the metal front electrode, for distance up to about *1.7 μm* from the metal strip edge.

We evaluated the open circuit voltage V_{oc} of an hypothetical cell with the optimised front electrode described in previous lines. To this purpose, we measured the short circuit current I_{sc} at V=0 and the V_{oc} at I=0 illuminating a device point close to a stripe of the front electrode (at about *100 nm* of distance). Moreover, I_{sc} and V_{oc} are connected by the well-known photovoltaic relation [6]

$$V_{oc} = nV_{th} \ln\left(\frac{I_{sc}}{I_s}\right)$$

where I_s is the saturation current of the diode, n is the ideality factor and V_{th} is the thermal voltage. Measured Voc values are in full agreement with the previous equation using the ideality factor of *1.1* and the saturation current density of ~ 10^{-21} *A/cm²*, as extracted from the forward characteristics not shown in figure.

Open Circuit Voltage Voc ~ *1 V* was obtained for an illumination current density of about 10^{-8} *A/cm²*, similarly to the one obtained in Ref.[1] using a p-n junction cell.

4. CONCLUSIONS

We have presented the EBIC measurements and analysis of an interdigit vertical Schottky diode proposed for beta-voltaic applications. The reduction of backscattered electrons fraction, using the interdigit front electrode structure, with respect to a standard continuous front electrode was demonstrated.

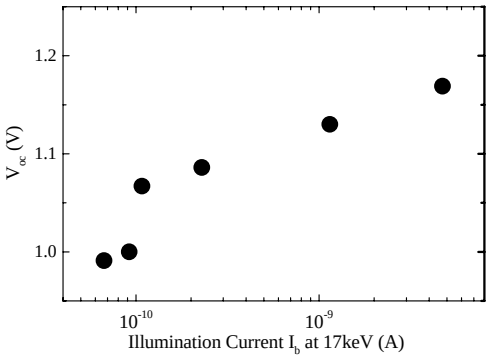

Fig. 2: Measured values of V_{oc} versus I_b at fixed beam energy of *17 keV*.

Short circuit current under irradiation with monochromatic electron beam was measured showing the advantages of the interdigit front electrode, opportunely designed in terms of higher short circuit device current. A relevant increase of beta-voltaic short circuit current with respect to a device with a continuous standard front electrode was achieved with this novel layout allowing to collect also low energy electrons. In particular, by irradiating the device with monochromatic e-beam of *17 keV*, an internal *Gain* 1.4 times higher than in conventional devices was obtained. Open Circuit Voltage of ~ *1 V* was obtained for an illumination e-beam current density of 10^{-8} *A/cm²*.

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SPIN PROPERTIES AND BALLISTIC TRANSPORT IN LOW-DIMENSIONAL AlGaN/AlN/GaN SYSTEMS

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ABSTRACT

In this work we investigated the electrical transport of AlGaN/AlN/GaN-based 2DEGs, a system particularly interesting for fundamental research on spin-orbit interaction and ballistic transport. Zero-field spin-splitting in the conduction bands was studied through magnetotransport experiments. The longitudinal resistivity measurements showed Shubnikov-deHaas oscillations. We developed a detailed analysis of the amplitude and phase modulation of the oscillations, which allows revealing the presence of two conductive channels, not detectable by standard analyses. The channels are identified as spin-split channels. Ballistic transport in 1D devices was also investigated; conductance quantization plateaus at $2e^2/h$ and $4e^2/h$ are found.

1. INTRODUCTION & EXPERIMENTAL

The development of novel electronic devices has triggered the investigation of various semiconductors materials, as gallium nitride (GaN) based heterostructures. Physical phenomena at the nanoscale, such as spin polarized currents or transport in ballistic regime, have been proposed as basis for new devices. GaN is investigated as a promising material for these purposes. However, the magnitude of the Rashba term contribution to the spin-orbit interaction in this system still needs to be investigated, and the high mobility needed for ballistic transport is not easily reached. In this communication, we report our results on these two issues.

A high mobility two dimensional electron gas (2DEG) with large sheet carrier density can be obtained in the AlGaN/AlN/GaN heterostructures without the use of doping because of the strong spontaneous and piezoelectric polarization in these materials [1]. Our sample was grown by MO-CVD on SiC substrate; the layer sequence consists of a 80 nm-thick AlN nucleation layer followed by a 1.8 μm-thick GaN buffer, a 2 nm-thick AlN exclusion layer and finally 23 nm-thick $Al_{0.23}Ga_{0.77}N$ layer. The heterostructure was passivated by depositing a 50 nm thick SiN layer using plasma enhanced CVD. We performed magnetotransport experiments with a standard low-frequency lock-in technique, at cryogenic temperature (base temperature 0.25 K), with a magnetic field perpendicular to the 2DEG with intensity up to 12 T.

2. SPIN SPLITTING IN 2DEG

Basic 2DEG characterization through classical Hall effect measurements shows that the carrier density and mobility at T=0.25 K are equal to 1.04 10^{17} m^{-2} and 2.2 m^2 V^{-1} s^{-1}, respectively. The values of longitudinal and transverse conductance as a function of the magnetic field intensity are compatible with the presence of a single conductive channel or multiple channels having similar conductivity and mobility differing by less than 10%.

At high fields, Shubnikov-deHaas (SdH) oscillations (Fig. 1) are well developed. From their frequency a carrier density of n=1.07 10^{17} m^{-2} is extracted, in agreement with the value evaluated by classical Hall effect data.

In SdH data, the presence of a spin-split subband is usually detected as a beating in the oscillations and as a split peak in its fast Fourier transform. These features are not observed in our curve. Nevertheless, the anomalous behavior of amplitude and phase of the oscillations as a function of B^{-1} reported in Fig. 2 suggests the presence of two parallel conductive channels. We remind that the SdH oscillations are expected to be exponentially damped because of the finite quantum mobility; in a logarithmic plot of the amplitude, such as the so-called Dingle plot shown in the upper panel of Fig. 2, a straight line is expected. We find instead a non-linear trend: in particular we find a change in the slope in the Dingle plot at about 0.22 T^{-1}.

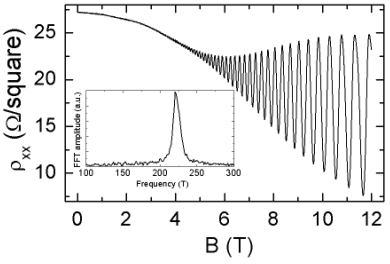

Fig. 1: Longitudinal resistivity as a function of magnetic field. Inset: FFT of the resistivity as a function of inverse magnetic field

Concerning the phase, it is expected to be constant at

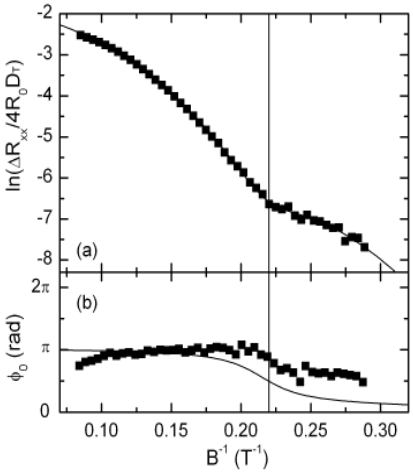

Fig. 2: (a) Dingle plot (the D_T term accounts for thermal damping)(squares) and data fit (line). (b) Residual phase of the SdH oscillations (squares); the continuous line is the calculated residual phase

a value of π rad, while we observe (Fig.2, lower panel) a sudden decrease, concomitant with the change in the slope of the amplitude. We have constructed a model that recovers both the change of the slope and the decrease of the phase by assuming the presence of two parallel conductive channels in the system, with slightly different mobility. In order to reproduce completely the data, a Gaussian damping is required. This functional dependence is explained assuming that the lineshape of the Landau levels is not Lorentzian, as in the standard model, but Gaussian. This lineshape is found when the correlation length of the mobility-limiting disorder is shorter than the de Broglie length of the electrons [2]. We checked this condition by comparing the transport parameter extracted from the measurement with those of a model simulating the roughness dominated disorder [3,4].

As for the identification of the nature of the two channels, we found that the presence of a spin-split conduction subband is the only possible mechanism compatible with both SdH effect and classical Hall effect data. The extracted value for the spin-splitting energy is ΔE=1.2 meV.

To compare this value with those reported in literature, we note that for samples having carrier density similar to our 2DEG spin splitting energies in the 0-13 meV range are reported [5,6]. This points out that the complicated spin-orbit interaction in wurtzite GaN systems is not yet fully understood, and that possibly other effects, such as different scattering mechanisms, can heavily affect the magnitude of this interaction.

3. QUANTIZATION OF CONDUCTANCE

The high mobility and high carrier density of the sample

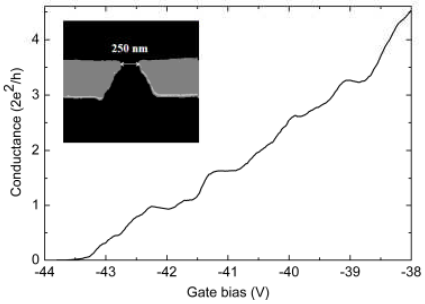

Fig. 3: Linear conductance of the quantum point contact. Inset: scanning electron microscopy of the device

implies a long mean free path (1.2 μm) and thus allows ballistic transport experiment. We fabricated 1D devices combining electron beam lithography, lift-off and reactive ion etching techniques. The devices are quantum point contacts with a split-gate geometry in which the 1D channel is obtained by biasing two lateral gate electrodes.

We have measured the linear conductance in several quantum point contacts: we found that the conductance is quantized and plateaus at the quantized values of $G_0=2e^2/h$ and $2G_0$ are present [7]. However, in some devices, signatures of the scattering from impurity are present in the curves. An example is shown in Fig. 3, in which a linear conductance measurement taken at 0.4 K is reported as a function of gate voltage taken in the QPC device shown in the inset. Plateaus are present, although their conductance value is not at regular quantized values. In particular, we note plateaus at G_0, 1.7 G_0, 2.7 G_0 and 3.3 G_0. Thus we find a regular spacing of G_0 for the first and the third plateau, while the second and the fourth have a reduced spacing of about 0.7 G_0. This behavior can be compatible with the presence of a scattering centre in the 1D channel whose spatial position affects mainly 1D propagating modes with odd electron wave functions [8].

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DIELECTRIC RELAXATION OF TRANSPARENT CONDUCTING OXIDES AT MICROWAVE FREQUENCIES

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ABSTRACT

The complex permittivity of non-percolating mica platelets, coated with antimony-doped tin oxide (ATO), was measured in the frequency range 100MHz – 8.5GHz using a coaxial reflectance probe. Relaxation peaks not normally seen for conductor-insulator composites at microwave frequencies were observed. Such relaxation phenomena are shifted from optical frequencies down to microwave frequencies in dielectric materials with coatings of intermediate conductivity. A series of composite samples was annealed at temperatures between 650°C and 900°C, and these exhibited a relaxation frequency which shifts from below 1GHz to above 4GHz with increasing annealing temperature. Samples with a higher concentration of platelets exhibited increases in both the real and imaginary permittivity. The relaxation frequency remained consistent with the temperature at which the sample was annealed, effectively demonstrating the ability to tailor the dielectric properties of these composite materials.

1. INTRODUCTION

Knowledge of the dielectric behaviour of conductor-insulator composites provides the opportunity to tailor the electrical properties of materials, with the prospect of many related applications such as frequency selective absorbers and improving heat transfer in microwave heating applications. Transparent conducting oxides (TCO) exhibit intermediate levels of conductivity which are above those of conventional doped semiconductors, but below those of metals [1]. To assist in the understanding of the relation between the microstructure and the macroscopic dielectric properties, in this work the complex permittivity of mica platelets coated with antimony-doped tin oxide (ATO) has been measured in the frequency range 100MHz – 8.5GHz using a coaxial reflectance probe. Dielectric relaxation is often observed in conductor-insulator composites at very high (e.g. optical) frequencies, but in core-shell structured materials such as those encountered here relaxation is shifted down to microwave frequencies and is caused by an interfacial polarization of the Maxwell-Wagner type.

2. EXPERIMENTAL DETAILS

The coaxial probe technique has been established over the last 30 years or so as a standard tool for evaluating the electrical properties of various materials in the microwave frequency range [2,3]. It is fast, non-destructive and requires little in the way of sample preparation. It involves the termination of a short length of flanged coaxial transmission line with the material under test, followed by measurement of the voltage reflection coefficient S_{11} at the interface with the material. A schematic diagram of the novel miniaturised coaxial probe used in our studies is shown in Fig. 1, based on an Anritsu K-connector (here K102F), which has an inherent bandwidth from DC up to 40 GHz. The connector's glass bead provides a convenient coaxial aperture, which can be ground flat and then polished using fine emery paper. The probe's inner and outer radii are a = 0.15mm and b = 0.80mm, respectively. Hence the aperture remains electrically small (i.e. wavelength much larger than $b - a$) over the full range of measurement frequencies (up to 8.5 GHz). Degeneratively-doped ATO layers were deposited by a sol-gel process, giving rise to a uniform coating of ~20nm thickness, on mica platelets 20-30μm in length, of typical platelet thickness 300nm. Non-conducting silica (SiO_2) and titania (TiO_2) outer layers are deposited to prevent percolation effects between the platelets and lastly the coated platelets are dispersed in a solvent based lacquer, based on a polyacrylate and nitrocellulose mixture. A schematic diagram of the resulting composite is shown in Fig. 2. To investigate the effects of increasing annealing temperature and particle concentration, the platelet particles were first annealed for 30 minutes at 650°C, 700°C, 750°C, 800°C, 850°C and 900°C. The samples are prepared for measurement by dispersing the coated particles in a lacquer at volume concentrations of 2%, 2.7% and 3.3%, and are spread to a thickness of around 50 μm onto 100 μm thick PET sheets (of low dielectric loss) and cured. The resulting dry volume concentrations are 12%, 14.5% and 16.6%. These thick film samples were then pressed against the aperture of a coaxial reflectance probe, as shown schematically in Fig. 1. It is essential that the sample is flat and is in intimate contact with the aperture, which is ensured by the plastic clamping screw shown. Measurements of the voltage reflection coefficient S_{11}were taken in the range 100MHz to 8.5GHz using an Agilent ENA 5071B Vector Network Analyser (VNA). The calibration plane is shifted to the aperture plane by first measuring the probe without the sample and then using this to normalize the sample data. The complex permittivity of the sample was calculated using a simple inversion process based on a capacitive aperture admittance model (for more details see [4]).

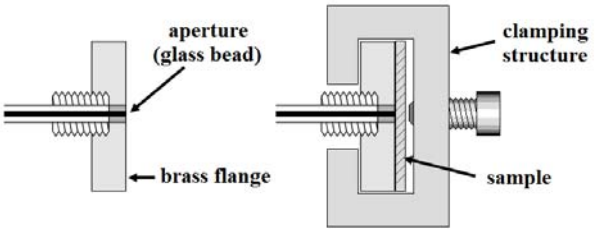

Fig. 1: Schematic diagram of the coaxial probe and sample fixture.

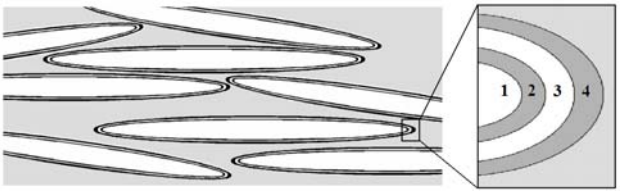

Fig. 2: Schematic diagram of the sample microstructure. (1) Mica, (2) ATO, (3) SiO_2, (4) TiO_2.

3. RESULTS AND DISCUSSION

Fig. 3 shows the real and imaginary permittivity of eighteen samples over the frequency range 100MHz to 8.5GHz. Three distinct data sets can be seen in the results, each corresponding to specific concentrations of particles. Within each of these are six plots corresponding to annealing temperatures between 650°C and 900°C (in steps of 50^0C). For each concentration of particles, the relaxation frequency is observed to increase with increasing annealing temperature. For fixed annealing temperature, the real and imaginary parts of the permittivity are both observed to increase with increasing particle concentrations. In this way it is possible to tailor the response of such composite materials by varying both the particle concentration and conductivity of the coatings (the latter changing the relaxation frequency). Note that though the concentration of particles in the samples in this work only reaches 16.6% by volume, higher concentrations (and therefore higher permittivities) are achievable without percolation because of the insulating outer layers. The dielectric relaxation observed in Fig. 3 indicates clearly the presence of a polarisation mechanism without significant low-frequency dispersion. Small conducting particles often exhibit increased absorption at higher frequencies, but the conductivity of the particles would have to be much reduced to achieve this at microwave frequencies. Dielectric relaxation has been reported at microwave frequencies for core-shell structures with a metallic outer shell, but having a thin-film related reduction in conductivity [5]. In this reported work the conducting layer is composed of a degenerately-doped semiconductor giving high levels of control over the conductivity (i.e. relaxation frequency) of the particles.

4. CONCLUSIONS

Investigations of the broadband frequency responses of conductor-insulator composites with core-shell structures have shown that for higher annealing temperatures (up to

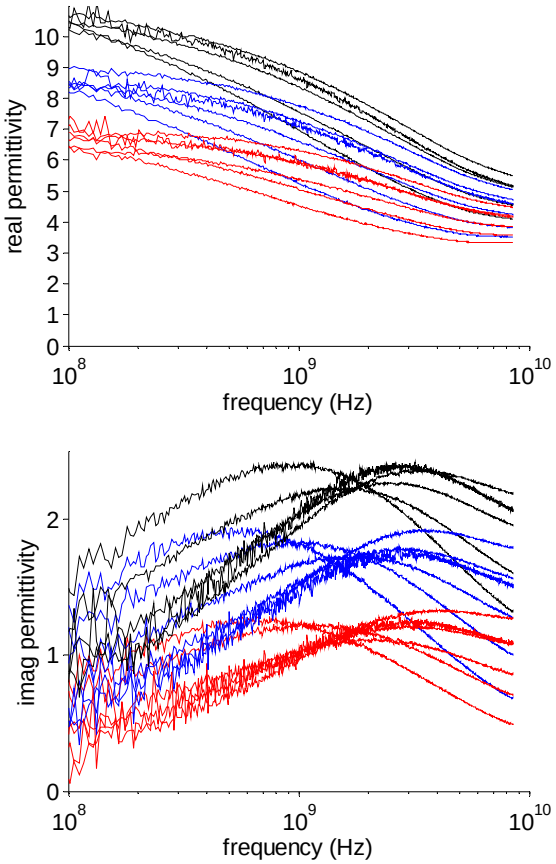

Fig. 3: Broadband measurements of the real (top graph) and imaginary permittivity of three sets of samples, corresponding to conducting particle volume concentrations of 12% (red), 14.5% (blue) and 16.6% (black). Each set includes six samples annealed at 650°C to 900°C.

900°C), the increased conductivity causes relaxation to shift upwards in frequency. In conventional materials one might expect dielectric loss to change proportionally with conductivity, but in composites such as these the dielectric loss at any given frequency may increase or decrease with higher annealing temperatures depending upon which side of the relaxation peak the measurements are made. Investigations also show that for an increased mass concentration of particles, increases in the real and imaginary permittivity of the material are observed. This demonstrates that the frequency and magnitude of relaxation may be controlled independently by annealing temperature and concentration of particles, respectively.

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HIGH CAPACITANCE DENSITY CAPACITORS BASED ON CALCIUM COPPER TITANATE THIN FILMS GROWN BY MOCVD

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ABSTRACT

Metal-Oxide-Metal planar capacitors based on $CaCu_3Ti_4O_{12}$ (CCTO) thin films, grown by Metal-Organic Chemical Vapor Deposition (MOCVD) and possessing a "bricks wall" morphology, have been fabricated and characterised. In these capacitors, the coexistence of two Maxwell-Wagner related phenomena has been demonstrated and modelled. A high reliability and reproducibility in CCTO capacitors can be achieved when all the phenomena are controlled. A remarkable high capacitance density (about 100 nF/mm^2) has been obtained at room temperature in optimised processing keeping low loss values ($\tan\delta < 0.1$).

1. INTRODUCTION

The electrical properties of $CaCu_3Ti_4O_{12}$ (CCTO) ceramics and single crystals received considerable attention due to the effective huge permittivity (up to 10^5) measured in the radio frequencies range, furthermore stable in the 100-400 K temperature range.[1] In the recent literature, this giant permittivity has been commonly related to extrinsic effects, i.e. not associated to the bulk material property itself. Therefore, the origin of the huge permittivity, arising from the capacitive response before the observed relaxation, has been mainly attributed to an internal barrier layer capacitor (IBLC) behaviour associated with insulating grain boundaries and semiconducting grains structure. This explanation has been corroborated by the imaging the insulating barriers at the grain boundaries of CCTO ceramics by Scanning Probe Microscopy (SPM) with conductive tips.[2,3]
However, for microelectronics applications, CCTO thin films are much more interesting than ceramics, thus for those applications the occurrence and the origin of the high permittivity deserve to be reliable demonstrated and studied specifically in thin films. In this context, it should be noted that the IBLC model cannot be responsible for the giant permittivity observed in CCTO single crystals[4] as well as in columnar thin films[5] where no grain boundaries are crossed between the two planar electrodes parallel to the surface.
Recently, it has been demonstrated the coexistence of both the internal barrier layer and the electrode polarization effects in CCTO ceramics.[6] In fact, both mechanisms can explain the "giant permittivity" observed in a wide range of frequencies (10^2-10^7 Hz). The dominant effect depends on the resistance associated to the grain boundaries, which is affected by the processing conditions.[7]
In this paper, we report on CCTO thin films deposited by Metal-Organic Chemical Vapor Deposition (MOCVD) possessing a "bricks wall" (BW) morphology and a giant permittivity.[8] In this case the two contributions, i.e. IBLC effect and Schottky barriers at the electrodes, can also be simultaneously present. Here, we demonstrate their occurrence and we evaluate the necessary conditions for a producible achievement of huge capacitive density in CCTO integrated condensers.

2. RESULTS

Capacitance vs. frequency (C-f) curves have been measured in the 10^2-10^6 Hz range and at different temperatures from 298 up to 473 K. Typical capacitance versus frequency curves (fig 1a) and tan δ response (fig 1b) have been collected at several temperatures and both point out to a peculiar temperature dependent relaxation behaviour: the relaxation frequency increases upon the increasing temperature. This trend, observed by macroscopic measurements, is similar to that found in CCTO ceramics.
The present CCTO films possess a "brick wall" (BW) structure with conducting grains surrounded by insulating grain boundaries, thus prompting to consider the IBLC model as a possible explanation for the observed temperature dependence of the relaxation frequencies.[7]
On the other hands, optimising the Schottky barrier of the top electrode in order to improve the metal/CCTO barrier a modified electrical behaviour is observed. It has been already demonstrated that a metal/semiconductor barrier can be optimised by rapid thermal processes (RTP) improving the dielectric performances. Detailed studies on the optimisation of the required thermal process on CCTO are reported elsewhere. Figure 1 shows the C-f characteristics (1c) and the tanδ (1d) at different temperatures after an RTP at 673 K for 60 seconds in Ar ambient. All the curves collected at different temperatures seem to shift to a unique and highest capacitance value which remains constant in the entire frequency range. A relaxation probably occurs at higher frequencies (~ 10^7 Hz) on the basis of the data reported in literature for PLD CCTO films.[5] Anyway, a stable response is obtained up to 1MHz. Therefore, after the RTP, a change of the physical phenomenon inducing the main relaxation occurs.

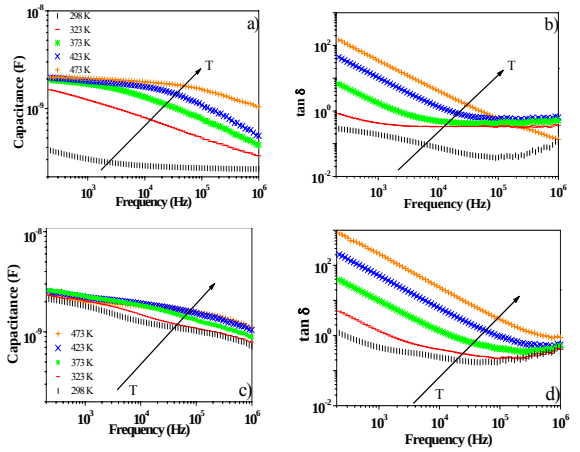

Fig.1: C-fs curves (a) at different temperatures on the as-fabricated Pt/CCTO/IrO_2 capacitor and their tanδ (b). C-fs curves (c) at different temperatures on the sample after RTP and their tanδ (d).

3. DISCUSSION

The fabrication of "bricks wall" CCTO thin films encourages the analogy with the CCTO ceramics. Both the presence of a temperature relaxation frequency dependence (fig. 1a) and the presence of insulating grain boundaries surrounding conducting grains urges the use of the IBLC model to explain the giant permittivity response in thin films.[7]

On the other hand, it has been strongly accepted in the literature reporting on metal-semiconductor barriers the processing dependence of the Schottky barrier (SB) properties. Non ideal and non homogeneous barriers arise low barrier values far from the ideal and reliable SB needed in device fabrication. One of the most fruitful method to improve the ideality of the SB is the use of post-metal deposition thermal processes in order to reduce the native non homogeneity and improving the quality factor (according to the thermo-ionic emission conduction mechanism).[7]

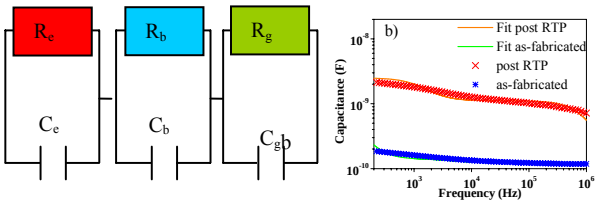

Fig.2: Equivalent circuit (a) used for the fitting of the experimental data. C-fs (b) before and after the RTP at room temperature and relative fitting curves.

It can be argued that the SB is only formed at the top electrode and not at the bottom, because of the huge thermal budget (1023 K for 180 minutes) inducing the formation of an ohmic contact at the bottom electrode/CCTO interface during the deposition.

This behaviour can be described using an equivalent circuit consisting of three parallel RC elements connected in series and respectively associated with the bulk, the grain boundaries and the electrode responses (see schematic in Fig. 2a). It can be accordingly modelled by the analytical solution of the capacitance response equations.

The main results coming from the simulation is the successful fitting of the data by the combination of both the IBLC and the electrode effects.

On the as-fabricated sample, due to the low SB efficiency (considering the thermo-ionic model; both the SB height and the ideality factor), only the IBLC effect deserves to be considered. By improving the SB efficiency, the C_e increases (see equation 4) and the electrode effect becomes dominant. The consequence is a more stable C-f response in a wider temperature range (see fig. 1c) maintaining a low dielectric loss (see fig. 1d where tanδ is <1 at frequencies higher than 100 Hz at room temperature).

Finally, it is noteworthy that remarkable high capacitance density (about 100 nF/mm^2) can be achieved at room temperature with a reasonable low dispersion factor (tanδ <1 at 1 MHz) and in a wide frequency range (10^2-10^6 Hz) if SB at the top electrode is optimised. This capacitance response of the CCTO based capacitor, independently if it is due to intrinsic or extrinsic effects, can be used in radiofrequency applications and open to the applicability of CCTO based condensers in integrated circuits.

4. CONCLUSION

CCTO thin films presenting a "bricks wall" structure have been fabricated by MOCVD. Two main mechanisms have been proposed for the explanation their extrinsic giant permittivity response. The coexistence of two Maxwell-Wagner mechanisms, i.e. IBLC effect and electrode polarization, has been demonstrated and modelled. The detailed description of the involved mechanisms could provide a clear picture of the factors to be controlled in order to obtain a high reliability and reproducibility in capacitors based on CCTO deposited films. Remarkable high capacitance density (about 100 nF/mm^2) can be achieved at room temperature with a reasonable dispersion factor (tanδ <1 at 1 MHz).

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INVESTIGATION OF THE BEHAVIOR OF BARIUM STRONTIUM TITANATE MOS CAPACITORS

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ABSTRACT

Barium strontium titanate (BST) capacitors were fabricated using pulsed laser deposition (PLD). A physical model was developed to describe the device characteristics. Simulation data from the model were compared with the experimental data, and the device physical parameters, as a function of the applied voltage, were obtained. By analyzing the data, the causes of the deviation from the ideal characteristics were identified. The study provides the knowledge needed to fabricate capacitors with optimized performance.

1. INTRODUCTION

Barium strontium titanate (BST) is one of the promising oxides that have a great potential for building many devices such as: metal-oxide-semiconductor field effect transistors (MOSFETs), RF microstructures, and high value capacitors. The characteristics of BST MOS capacitors depend on many factors. Among these factors are the deposition technique and growth parameters of the BST layer, the fabrication process of the capacitor, and the quality of the interfacial layer between the BST and the semiconductor. To be able to identify these factors and know how they affect the capacitor performance at different frequencies, we prepared capacitors with different fabrication processes and developed a model that can describe their performance. By comparing the results from the experimental measurements and the model calculations, we were able to identify the causes of the performance deviations.

2. DEVICE FABRICATION

Three sets of capacitors, named samples BST 25, BST 26, and BST 27, were fabricated using pulsed laser deposition (PLD) on n-Si wafers with a doping of 7×10^{14} cm^{-3}, 2×10^{16} cm^{-3}, and 8.2×10^{14} cm^{-3}, respectively. The deposition was performed at 900°C with laser frequency of 30 Hz and 3000 pulses. Oxygen pressure was set to 1, 10, and 75 mT for the above samples, respectively. The energy for BST 25 and BST 26 was set to 300 mJ but was reduced to 150 mJ for BST 27. Thicknesses of the BST films for the devices used in this study were found to be 256 nm, 290 nm, and 77 nm for BST 25, BST 26, and BST 27, respectively.

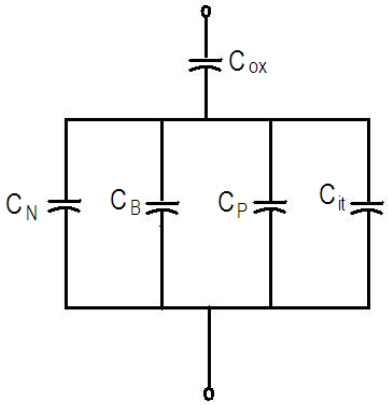

Fig. 1: Equivalent circuit diagram of MOS capacitor under bias voltage [1].

3. MODELING

The model used in this study took into account all capacitive components of the structure, as shown in Fig. 1. In this model, C_{OX} is the capacitance of the BST layer in series with the capacitance of the10 Å naturally grown SiO_2 layer; C_N is a result of the electron accumulated during the accumulation region; C_B is the bulk capacitance due to the depletion region under the oxide layer; C_P is a result of the hole inversion layer during inversion mode; and C_{it} is a result of the charges accumulated at the interface. The C-V characteristics were measured and simulated for the accumulation, depletion, and inversion regions at 1kHz and 1 MHz.

4. RESULTS AND ANALYSIS

The forward and reverse sweeping curves at 1 kHz for the three samples are shown in Fig. 2, Fig. 3, and Fig. 4. As can be seen from the figures, the shapes of the curves are different, which are attributed to the differences in the growth parameters for each sample. The theoretical data obtained from the model was found to coincide with the experimental data as shown in reference [2].

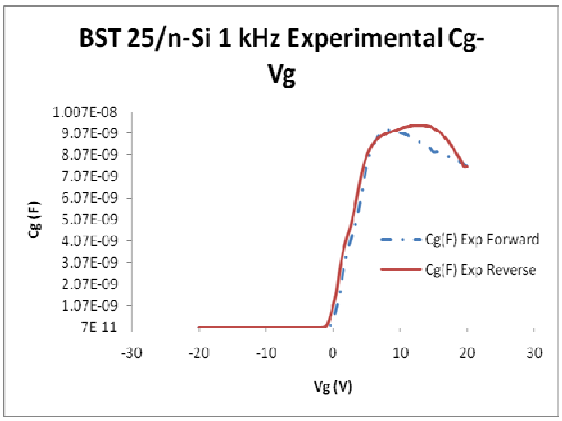

Fig. 2: C-V curve for BST 25 at a frequency of 1 kHz

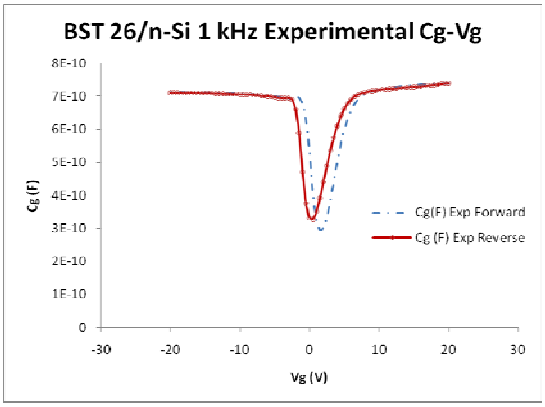

Fig. 3: C-V curve for BST 26 at a frequency of 1 kHz

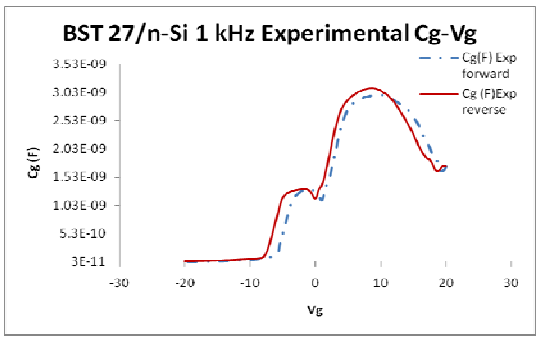

Fig. 4: C-V curve for BST 27 at a frequency of 1 kHz

Fig. 2 shows that in the accumulation region (in this case at positive voltages), the capacitance decreases with V_g. This indicates that the capacitance in this region is voltage-dependent. This anomalous behavior of the C-V curve is mainly due the leakage current in the dielectric [3]. Our conductance-voltage (G_p-V_g) measurements support this assumption. The hysteresis effect in the accumulation region may be a result of positive deep traps at the semiconductor-oxide interface for this sample. In the forward sweep electrons at the interface are swept to the gate and the positive traps are stripped from their electrons causing a larger reduction of the effective charge ΔQ and in the capacitance. When the voltage decreases, during the reverse sweep, the traps capture their electrons and get neutralized increasing the effective number of negative charges and consequently the capacitance.

Fig. 3 shows a hysteresis in the depletion region. Again, the cause of the hysteresis is due to the depletion and repopulation trap centers at the interface of the oxide and the semiconductor [4]. The negative traps (electrons) cause a clockwise hysteresis loop, whereas positive trapping induce a counterclockwise hysteresis loop [4-5]. The figure shows also that the capacitance in the inversion layer increases to the value of the accumulation region. This behavior is due to the fact that the minority carrier response time is smaller than the period of the a.c. signal.

Fig. 4 shows that, in the accumulation region, the capacitance decreased with V_g. Again this is attributed to the leakage current from the gate to the semiconductor [3, 6]. The existence of the leakage current has been confirmed from the G_p-V_g measurements. As in the case of sample BST 25, the hysteresis effect in the accumulation region for BST 27 may be a result of the deep traps at the semiconductor-oxide interface and in the oxide, but in this case it appears that the traps are negatively charged. Fig. 4 also shows a distortion in the C-V curve from 2V to -6V for the forward sweep and from 0V to -8V for the reverse sweep. This region is the transition from the depletion region to the inversion region. It is believed that this distortion corresponds to effects of donor type traps, as explained in reference [6].

The three samples were also measured at 1 MHz. The C-V curves at 1 MHz were found to be identical to the curves at 1 kHz, shown in Figs. 2, 3, and 4. In other words, the C-V characteristics do not change with the variation of frequency. This shows that the material properties, such as the minority carrier response time or trap density, do not change with the frequency either. The high leakage current through the BST suggests that the type of charges in the oxide is negative, and the density is high. This is confirmed by the fact that the direction of the shift between the forward and reverse bias sweeping is always to the left [2,4].

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AlGaN ULTRATHINNED 2DEG STRUCTURES FOR NO_x SENSING

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ABSTRACT

A normally-off HEMT with an open gate layout is fabricated by etching down the AlGaN layer. The reaction of NO_x with the gettered surface water changes the charge polarity which changes the 2DEG conductivity immediately. At 84% relative humidity and 500 ppb NO_2 the 2DEG conductivity decreases by factor of 500. The absolute noise level of the current is smaller than 20 pA, resulting in a signal-to-noise ratio of 10^5. Concentration steps of 1ppb NO_2 are reproducibly detected. The sensor allows to monitoring the NO_x concentration in the air (1 - 50 ppb) at humidity levels down to 10%.

1. INTRODUCTION

The most sensitive devices for gas monitoring developed recently are based on carbon nanotubes (CNT), two dimensional electron gas (2DEG) or grapheme. The CNT and grapheme technologies are still rather complicated showing lack of long term stability. In contrast 2DEG based devices offer the same sensitivity combined with much higher life time. The normally-off high electron mobility transistors (HEMT) are widely known within the group-III-nitrides electronics. The (2DEG) in the AlGaN based HEMT is completely depleted at a critical thickness of 4 - 6 nm and reversibly restored applying a positive gate voltage. The strong dependence of 2DEG conductivity on the proximal charge can be used for ultrasensitive chemical detection. In the work presented this phenomena is used for detection of NO_x gases in a sub-ppb range.

2. CONCEPT

To achieve significant improvement of the sensitivity, resolution, response time and to minimize the power consumption we utilize a sensitive open gate AlGaN area within the GaN/AlGaN hetero-junction of a 2DEG-based GaN-FET sensor. The sensor layout is shown in Fig. 1, where the AlGaN layer is ultrathinned down to 6 - 7 nm. The proposed concept enables an ultrasensitive detection and monitoring of NO_2 gas in ambient air without additional functionalization layer. The naturally gettered water on the AlGaN surface creates a positive charge zone. Upon the gas exposure, NO_2 molecules react with the water neutralizing this positive charge. As a consequence, a tremendous decrease of the charge carrier density (CCD) in the 2DEG is observed leading to decrease of the current flowing through 2DEG channel.

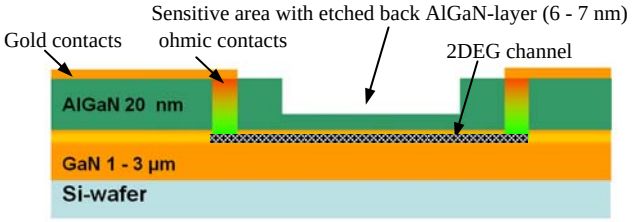

Fig. 1: Schematic layout of 2DEG-based sensor in a simple GaN-FET configuration with an open gate AlGaN sensing area back-etched to a thickness of 6 - 7 nm.

3. EXPERIMENTAL

The AlGaN/GaN layers are grown by MOVPE-technique. The sensor processing consists of three main steps: ohmic contact formation, channel patterning, and channel back-etching. The ohmic contacts were fabricated by a standard lift-off process, including deposition of 20 nm Ti/ 40 nm Al / 25 nm Mo/ 50 nm Au, followed by annealing at 800ºC in a nitrogen atmosphere. 2DEG-channels are formed and isolated from each other by etching of trenches into the GaN/AlGaN-material. The channel pattern was transferred into the 2DEG by reactive ion etching (RIE) using a chlorine based plasma. For the fabrication of the ultrathin 2DEG-channels, the AlGaN-layer was back-etched from an initial thickness of 22 nm down to 6 nm using the LOR5A-polyimide as a mask. A special ICP-RIE with a biased RF-power dry etching tool was utilized having an etching rate in the order of 1 nm/min. Due to epi-etch like process the surface roughness did not exceed 0.3 nm. The resulting current was measured at an applied voltage of 0.5 V.

4. RESULTS AND DISCUSSION

In dry N_2, the sensor with the 6 nm thick AlGaN layer was nearly in the switched-off state, having a device current smaller than 2 nA, due to a full depletion of the 2DEG-channel through the surface states an small piezoelectric polarization. In humid environment a naturally gettered water layer is formed on the AlGaN-surface inducing a positive space charge, which is equal to the effect of a positive gate potential, i.e. strongly increasing the conductivity of the 2DEG-channel. The device current reaches almost 1 µA at 84% RH. Fig. 2 shows the response signals of two sensors with different AlGaN thickness during exposure to 500 ppb NO_2.

The current of the sensor having a 6 nm AlGaN (dashed) decreases from the initial value of about 900 nA to about 2 nA, fully depleting the 2DEG.

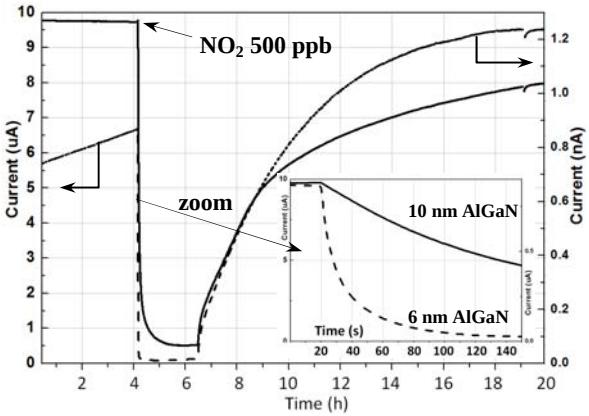

Fig. 2: Response of ultrathin 2DEG-channels with a 10 nm AlGaN layer (solid, left Y-axis) and with a 6 nm AlGaN layer (dashed, right Y-axis) to 500 ppb NO_2 in N_2 atmosphere at 84% RH

Its response dynamic is 10 times faster compared to the sensor with a 10 nm AlGaN layer (inset in Fig.2). The absolute noise level is smaller than 20 pA, providing a signal-to-noise ratio of 10^5. Assuming a linear sensor response, the minimum detectable NO_2 concentration within 1 min or 10 min after exposure are estimated to be 10 ppt and 1 ppt, respectively. The sensor with 10 nm AlGaN layer can be characterized by a considerably lower signal-to-noise ratio of 500 and an absolute noise level of 200 pA.

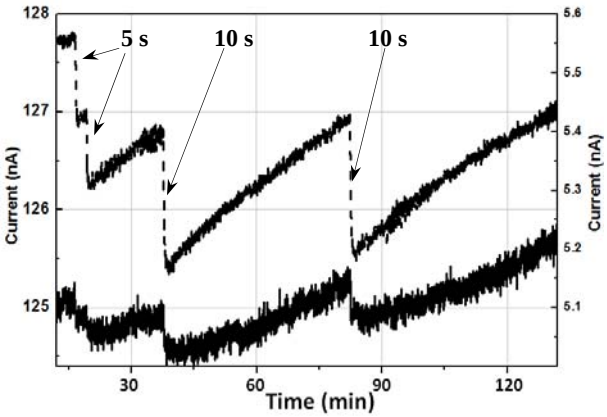

Fig. 3: Response dynamic of the sensors from Fig.2 to 5 s and 10 s pulses of 500 ppb NO_2 in synthetic air at 40% RH

The sensor response to 500 ppb NO_2 at 40% RH was measured in synthetic air using pulsed gas exposures of 5 s and 10 s (Fig. 3). The response to these short gas pulses can easily be distinguished with the sensor with 6 nm AlGaN layer (dashed) due to its high signal-to-noise ratio and fast response dynamic. Although oxygen reduces the baseline current considerably, it does not inhibit the sensor response. To determine the limit of detection and the resolution, the NO_2 concentration was reduced to 60 ppb (the minimum attainable with the experimental set) and increased in 1 ppb steps to 70 ppb. A humidity level of 38% was chosen as it corresponds to that of average ambient conditions. This measurement was performed again using N_2 as a carrier gas to prevent the influence of O_2. The results, shown in Fig. 4a indicate that the limit of detection is indeed far below 60 ppb while 1 ppb steps in the NO_2 concentration can easily be distinguished.

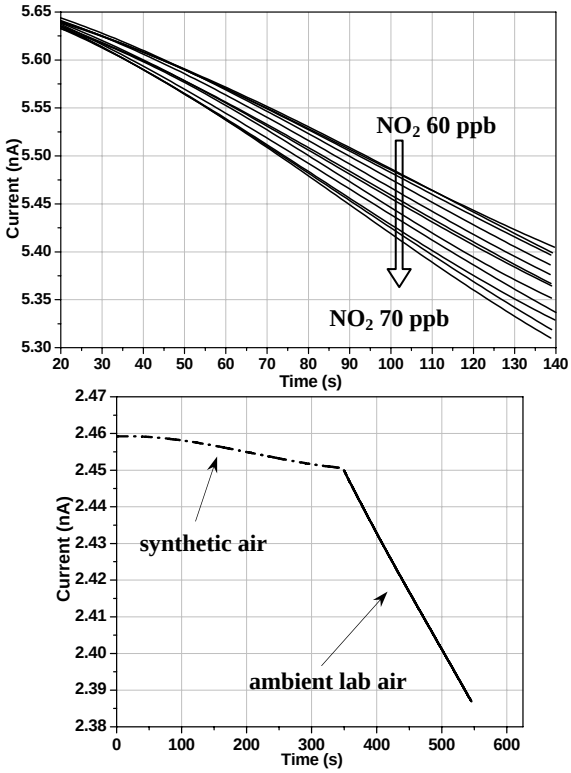

Fig. 4: a) Response to NO_2 concentrations in N_2 at 38 % RH ranging from 60 ppb to 70 ppb in 1 ppb steps b) Sensor response to NO_2 containing in normal ambient air (1 - 50 ppb)

Having established that the sensor operates at ambient conditions with a detection limit below 60 ppb, it should be possible to measure the NO_2 present naturally in ambient air (1 - 50 ppb). This is demonstrated in Fig. 4b. Firstly, the sensor was exposed to a flow of NO_2-free synthetic air at 38% RH, matching the relative humidity of room air. Next, the synthetic air flow was replaced by natural ambient air containing NO_2.

5. CONCLUSIONS

The results obtained indicate the feasibility of practical application of the sensor for continuous air quality monitoring. By tuning the AlGaN thickness the sensor can be operated in a full depletion or in a continuous gas exposure mode. This sensor can enable a low power continuous on-site air pollution monitoring.

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